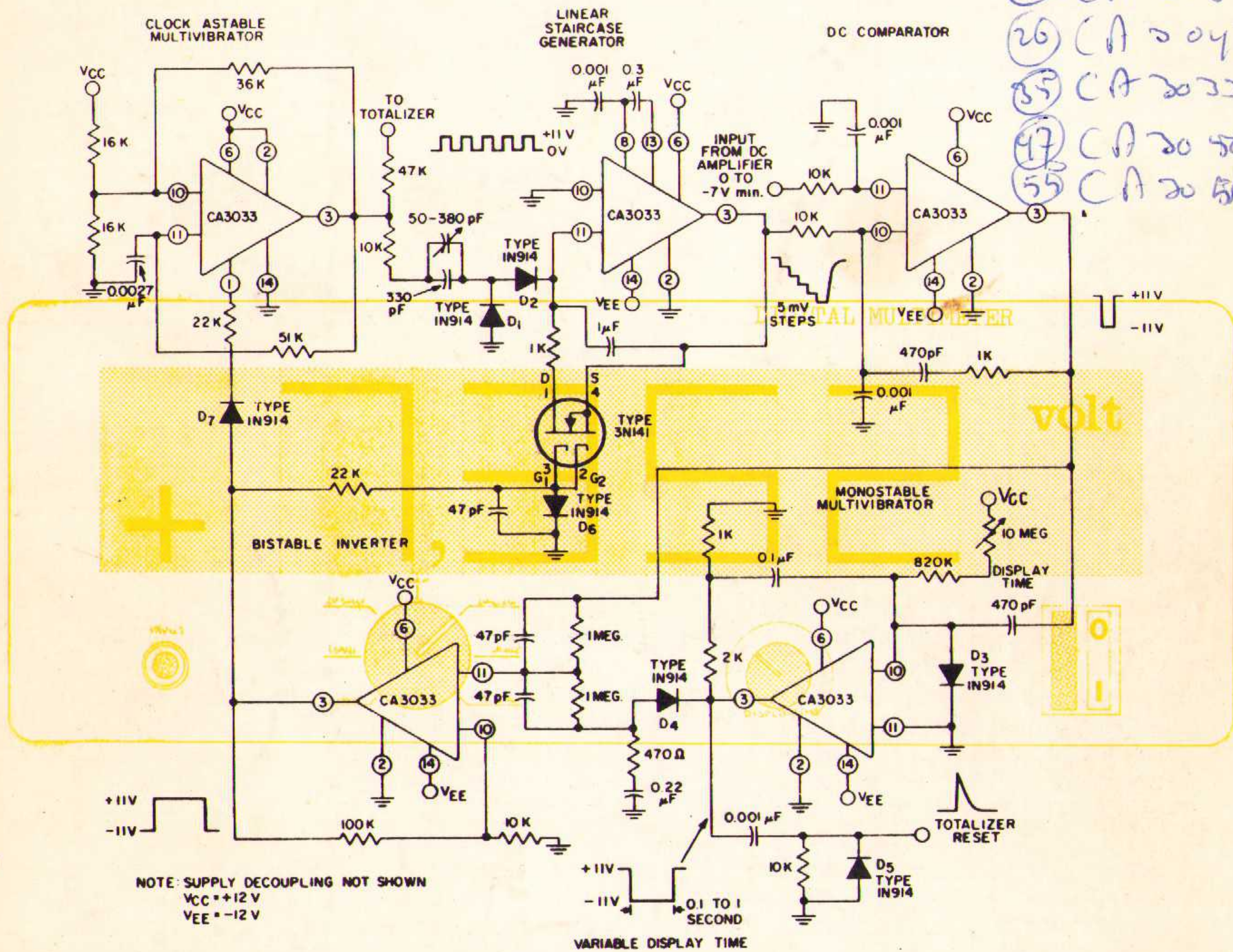


TECHNISCHE DOCUMENTATIE 1971

DEEL ① ② ③ 4 5 6 7 8 9 10 11 12

④ TMS 7B 3000
shift reg.
⑨ 7413 AN
②② CA 3035
②⑥ CA 3047
③⑤ CA 3033
④⑦ CA 3059
⑤⑤ CA 3059 AN



n.v. technische handelmaatschappij
van der
ELEKTRONICA

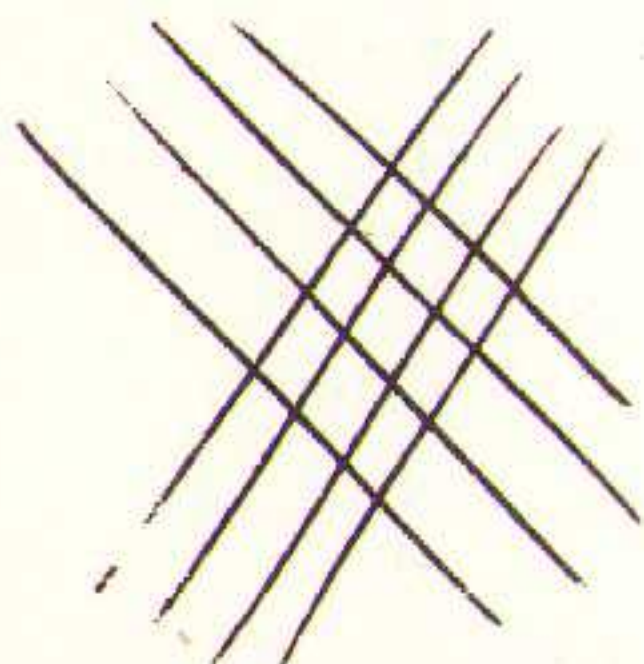
Snellemanstraat 10-11 bij Zwaanshals, Rotterdam - noord
 Telefoon: 010-240812-243497, administratie: 010-245516
 Giro: 295550. Bankrelatie: Amsterdam-Rotterdam Bank NV.
 Postorders en correspondentie: Postbus 3149 te Rotterdam
 Filiaal: Blasiusstraat 14-16 bij Ceintuurbaan, Amsterdam
 Telefoon: 020-947218.

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A T T E N T I E : M E L D I N G V A N V E R H U I Z I N G E N

Verhuizingen geven veel administratief werk indien alle benodigde gegevens ontbreken; met ingang van deze jaargang moeten wij aan het verwerken van Uw verhuizing strikt de volgende voorwaarden stellen:



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Bestellen op een moderne manier.

Mede dank zij onze voorraadpositie en levertijd maken steeds meer cliënten regelmatig gebruik van onze service. Wij hebben hierbij altijd getracht, onze service optimaal te laten functioneren en onze cliënten zo deskundig mogelijk te adviseren omtrent het toepassen en verwerken van de door ons aangeboden kwaliteitsartikelen. Dit is een bijzonder tijdrovende bezigheid, doch ook in de toekomst willen wij aan iedereen deze service verlenen en, waar nodig, nog verder uitbreiden. Daarvoor is echter Uw medewerking noodzakelijk!!!

Door het steeds intensiever gebruik van gegarandeerde betaalkaarten van de Post-, Cheque- en Girodienst en betaalcheques van de hier ter lande gevestigde bankinstellingen kunt U ons veel tijd besparen door Uw bestellingen op één van de volgende manieren te laten plaatsvinden. U bespaart hiermee al onze afdelingen tijd, hetgeen ter Uwer gunste tot uitdrukking komt in een optimale service, deskundig advies, snelle levertijd en (want: tijd is geld) een concurrerende prijs.

Manier 1. Bestelling door bijvoeging van een gegarandeerde betaalkaart van de PCGD.

Door de Nederlandse Post-, Cheque- en Girodienst worden zonder kosten betaalkaarten tot f 100,- per kaart verstrekt aan rekeninghouders, welke nimmer hun saldo overschreden hebben. Over deze kaarten kunt U inlichtingen verkrijgen bij elk PTT kantoor of het girokantoor te Den Haag of Arnhem. Deze kaarten worden tegenwoordig als betaalmiddel aanvaard en zijn reeds in het bezit van zo'n 1.500.000 rekeninghouders. Deze kaarten kunt U, voorzien van ons gironummer (295550), naam (N.V. Technische Handelmaatschappij Van Dam Elektronica), plaats (Rotterdam-3011) en Uw handtekening bij Uw bestelling voegen. Vult U hierbij echter op een kaart géén bedrag in: zou U door prijsfluctuaties of verzendkosten te weinig betaald hebben, dan kunnen wij Uw bestelling niet volledig in behandeling nemen en geeft dit voor U bijzonder veel ongemak! Bij Uw bestelling wordt door ons een volledig gespecificeerde nota gevoegd, terwijl op deze wijze U tevens de tegenwoordig bijzonder opgelopen rembourskosten (f 3,14) beperkt tot slechts f 0,50-f 0,80 voor pakjes tot 250 gram. Daarnaast heeft U Uw bestelling in huis op de werkdag, volgend op de dag, dat wij Uw bestelling ontvangen (dus 1 à 2 dagen nadat U Uw bestelling heeft gepost: adresseer hiertoe uitsluitend aan onze Postbus nr. 3149) en behoeft er niemand thuis te blijven om de postbode te betalen! U ontvangt op deze wijze Uw bestelling franco huis, terwijl U na circa 1 week de afschrijving door de Post-, Cheque- en Girodienst wordt toegezonden. Wij kunnen U op deze wijze een snelle service verlenen doordat onze orderafdeling en boekhouding geen remboursskaarten behoeven te verzorgen.

Manier 2. Bestelling door bijvoeging van een gegarandeerde bankcheque.

Ook door de Nederlandse bankinstellingen worden cheques verstrekt aan houders van een rekening-courant. Deze cheques zijn eveneens gegarandeerd tot f 100,-. Over deze betaalcheques kunt U bij Uw bankrelatie nadere informatie verkrijgen. Op deze cheques, welke U ook bij Uw bestelling kunt voegen, dienen onze naam (N.V. Technische Handelmaatschappij Van Dam Elektronica) en Uw handtekening te worden geplaatst. Ook hierbij dient U op één kaart geen bedrag in te vullen, zodat het juiste bedrag door ons kan worden ingevuld. De verdere afwikkeling van Uw opdracht vindt plaats als onder "manier 1." is aangegeven, terwijl U na enige tijd een afrekening van Uw bankrelatie ontvangt.

Manier 3. De kostbare manier voor levering onder rembours.

Kunt U geen gebruik maken van de onder manier 1 en 2 opgegeven mogelijkheden, dan kunnen wij Uw bestelling, mits het totaalbedrag boven f 15,- is, onder rembours uitvoeren; hierbij bent U aan verzendkosten f 3,14 of meer kwijt (dat vraagt de PTT nu eenmaal...), terwijl U voor bedragen onder f 25,- bovendien f 1,50 extra voor verpakkingskosten in rekening wordt gebracht. Vraagt U daarom ook een girorekening of bankrekening aan: het is zo gemakkelijk, het bespaart U geld en U krijgt nog rente ook

Wilt U Uw bestelling per expresse of aangetekend laten verzenden, dan kunt U dit bij Uw bestelling aangeven; de extra portokosten bedragen hiervoor f 1,25. Door ons gironummer en onze naam op Uw kaart aan te geven hebben deze voor buitenstaanders generlei waarde.

Wij zijn ervan overtuigd, dat de onder 1. en 2. aangegeven bestelmethode voor U en ons een groter gemak met zich mee zullen brengen en rekenen op Uw welwillende medewerking hierbij; uiteindelijk is dit ook in Uw voordeel

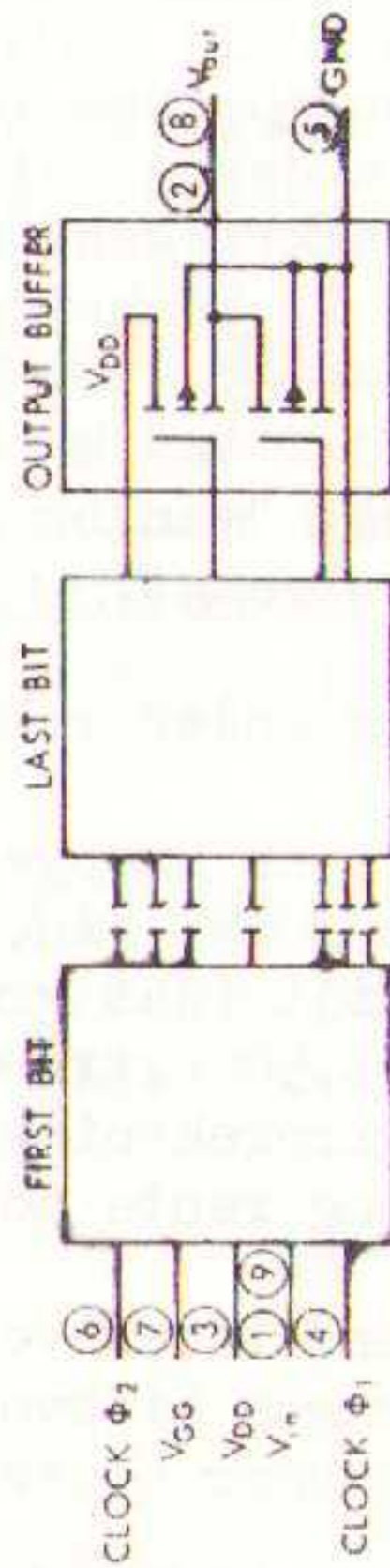
FOR OPERATION FROM DC TO 1 MHz

description

The TMS 7B 3000 LA consists of two separate 25-bit static shift registers with independent input and output terminals, and common clocks, power, and ground. Two power supplies and two external clocks are required for operation with a third clock generated internally. Cross-coupled flip-flops are used to implement each bit of delay, enabling data to be stored indefinitely between clock pulses. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-mode transistors.

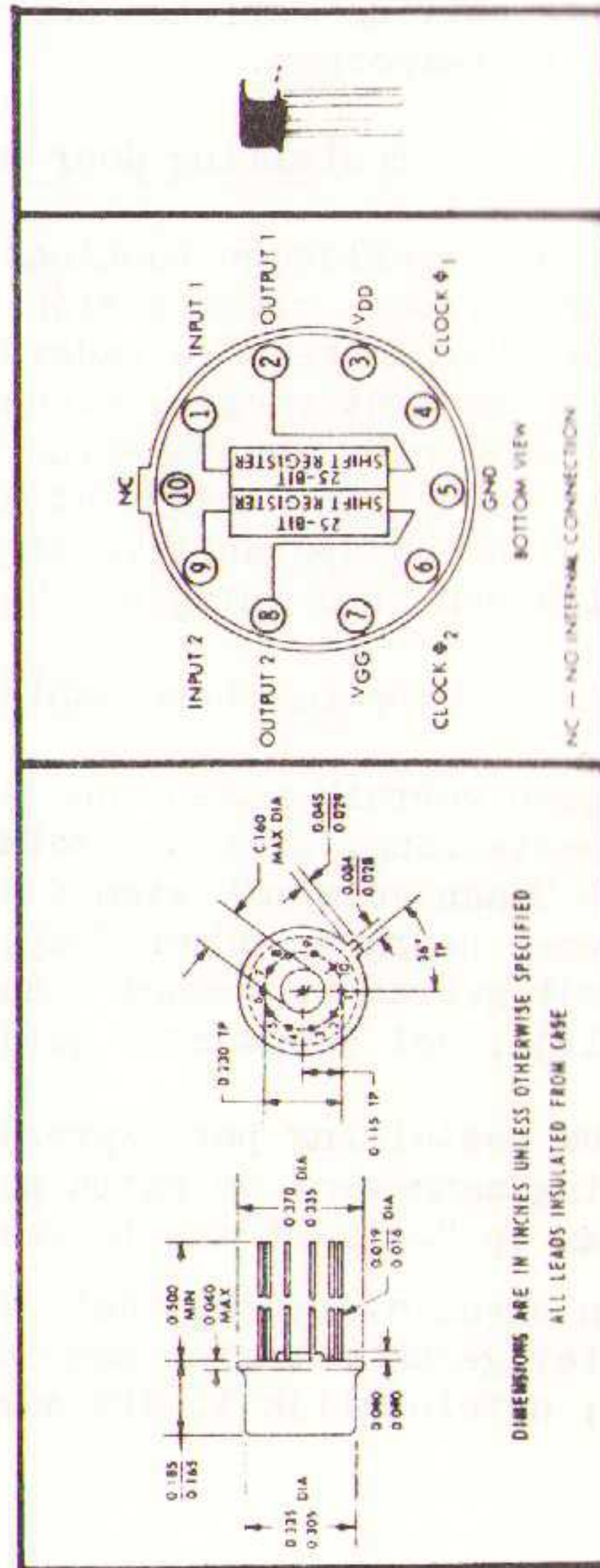
Transferring data into the register is accomplished when the Φ_1 clock is at a logical 1. Shifting the data occurs when the Φ_2 clock is momentarily pulsed to logical 1 and the Φ_2 clock to logical 0. For long-term data storage, the Φ_1 clock must be held at logical 0 and the Φ_2 clock must be held at logical 1. Output data appears on the negative-going edge of the Φ_2 clock pulse.

functional block diagram



mechanical data

The TMS 7B 3000 LA package outline is same as JEDEC TO-100 except for diameter of standoff.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	-30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	-30 V to 0.3 V
Clock and data input voltage ranges (See Note 1)	-30 V to 0.5 V
Operating free-air temperature range	-55°C to 85°C
Storage temperature range	-55°C to 150°C

NOTE: 1. These voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	-13	-14	-15	V
Supply voltage V_{GG}	-27	-28	-29	V
Width of data pulse, $t_p(\text{data})$ (See Figure 2)	0.4			μs
Width of clock pulses: $t_p(\text{clock } \Phi_1)$ (See Figure 2)	0.4		10	μs
$t_p(\text{clock } \Phi_2)$ (See Figure 2)	0.4			μs
Clock delay time, $t_d(\text{clock})$ (See Figure 2)	0.01		10	μs
Rise time of clock pulse, $t_r(\text{clock})$ (See Figure 2)			5	μs
Fall time of clock pulse, $t_f(\text{clock})$ (See Figure 2)			5	μs
Clock repetition rate	0		1	MHz

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at data input	-10			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at data input		-2		V
$V_{in(1)\phi}$	Input voltage required to ensure logical 1 at either clock input	-27			V
$V_{in(0)\phi}$	Input voltage required to ensure logical 0 at either clock input		-2		V
$V_{out(1)}$	Logical 1 output voltage	-11	-13		V
$V_{out(0)}$	Logical 0 output voltage	-0.3	-1		V
V_{out}	Output voltage	-10	-11		V
$I_{in(1)}$	Logical 1 level input current into data input	-5	-6		μA
$I_{in(1)\phi}$	Logical 1 level input current into either clock input	-50			μA
$I_{in(0)\phi}$	Logical 0 level input current into either clock input	40	60		k Ω
$Z_{in\phi 2}$	Clock Φ_2 input impedance	0.5	2		k Ω
Z_{out}	Output impedance	3	5		pF
C_{in}	Capacitance of data input	8	12		pF
$C_{in\phi}$	Capacitance of each clock input	-14	-20		mA
I_{DD}	Supply current into V_{DD} terminal	-2.0	-3.5		mA
I_{GG}	Supply current into V_{GG} terminal				

†Unless otherwise noted, $V_{DD} = -13$ V to -15 V, $V_{GG} = -27$ V to -29 V, $R_L = 10$ M Ω , and $C_L = 10$ pF.
‡Test applied values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from clock Φ_2 to data output See Figure 2		325	475	ns
t_{pd0}	Propagation delay time to logical 0 level from clock Φ_2 to data output See Figure 2		325	475	ns

timing diagram

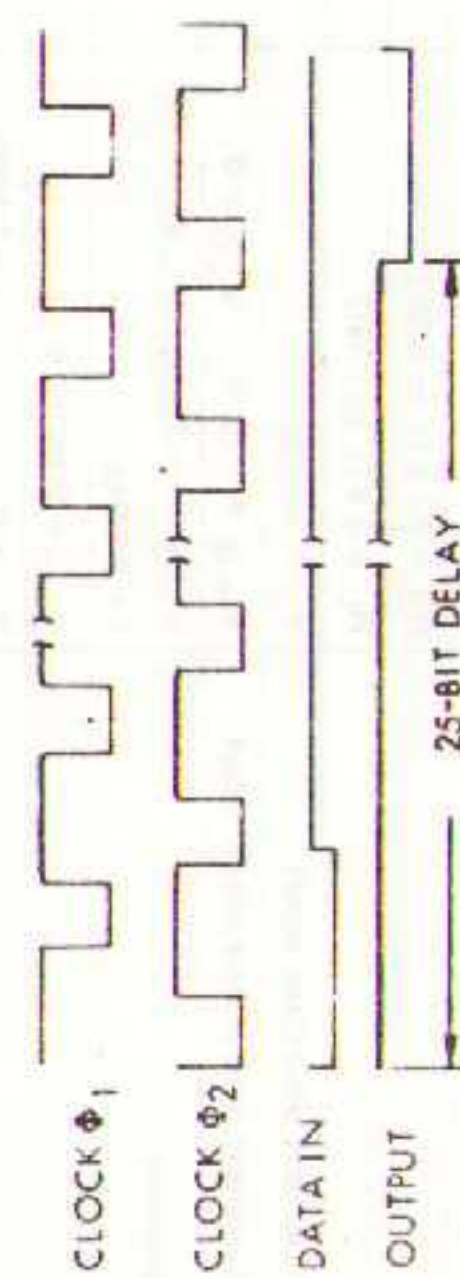


FIGURE 1

voltage waveforms

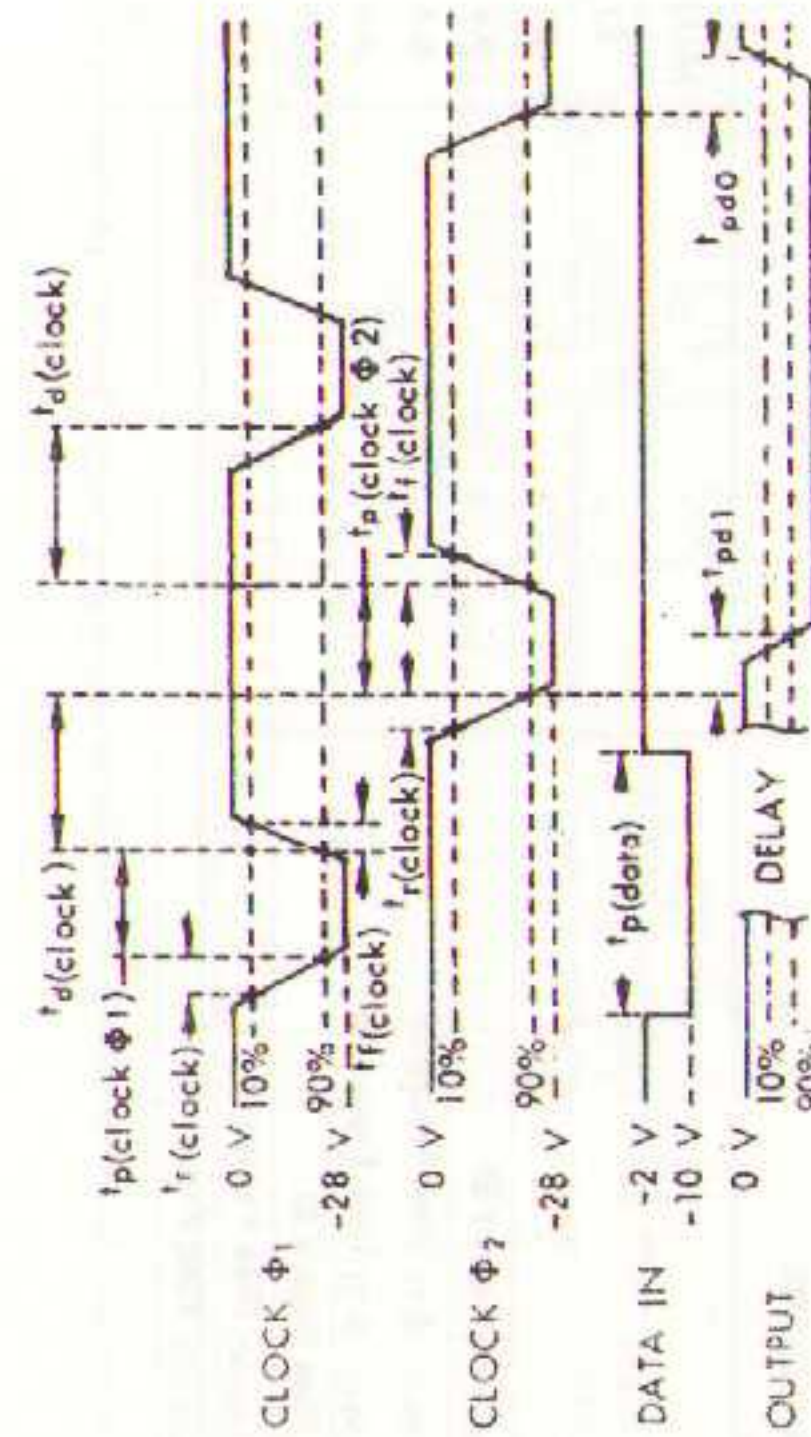


FIGURE 2

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.



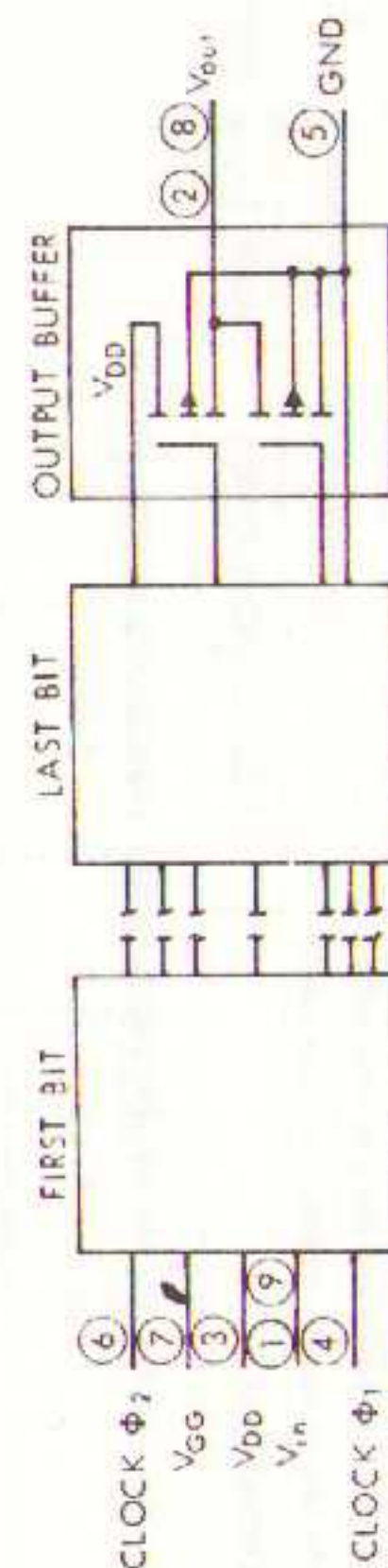
TEXAS INSTRUMENTS

description

The TMS 7C 3002 LA consists of two separate 50-bit static shift registers with independent input and output terminals, and common clocks, power, and ground. Two power supplies and two external clocks are required for operation with a third clock generated internally. Cross-coupled flip-flops are used to implement each bit of delay, enabling data to be stored indefinitely between clock pulses. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-mode transistors.

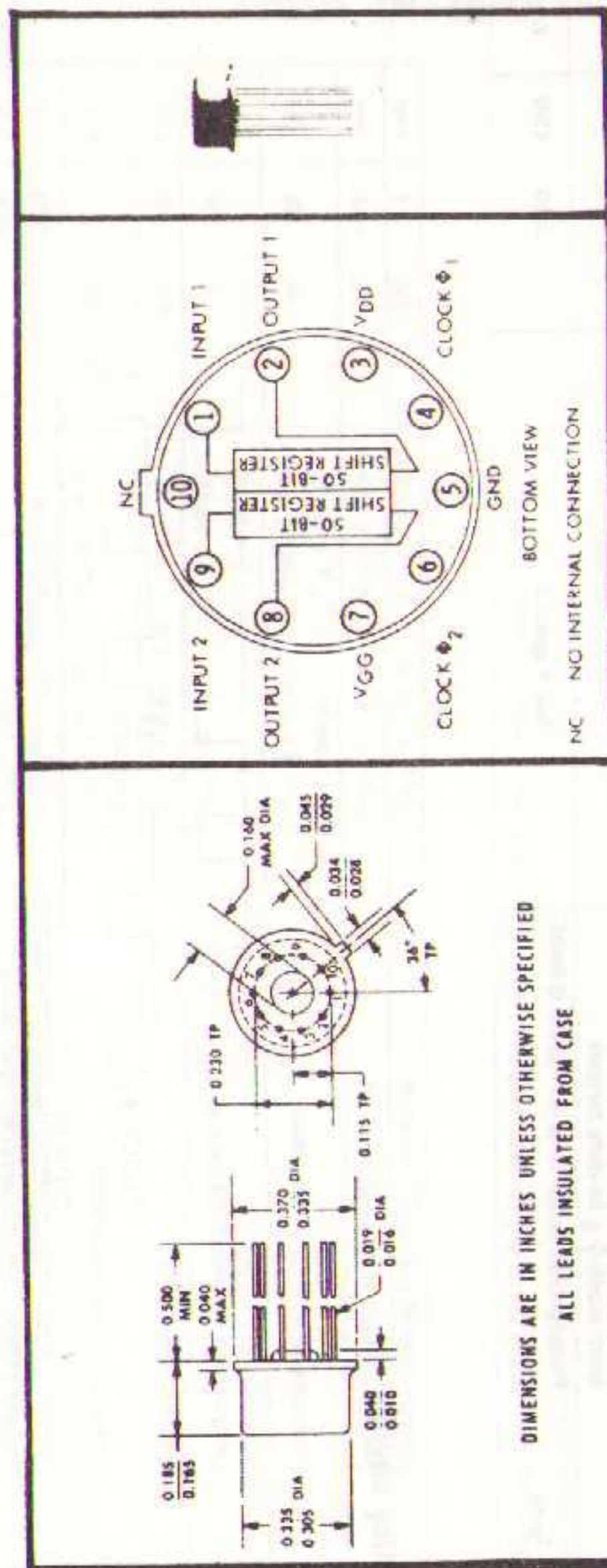
Transferring data into the register is accomplished when the Φ_1 clock is at a logical 1. Shifting the data occurs when the Φ_1 clock is momentarily pulsed to logical 1 and the Φ_2 clock to logical 0. For long-term data storage, the Φ_1 clock must be held at logical 0 and the Φ_2 clock must be held at logical 1. Output data appears on the negative-going edge of the Φ_2 clock pulse.

functional block diagram



mechanical data

The TMS 7C 3002 LA package outline is same as JEDEC TO-100 except for diameter of standoff.



DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
ALL LEADS INSULATED FROM CASE



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	-30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	-30 V to 0.3 V
Clock and data input voltage ranges (See Note 1)	-30 V to 0.5 V
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NOTE: 1. These voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	-13	-14	-15	V
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Width of data pulse, $t_{p(data)}$ (See Figure 2)	0.4			μ s
Width of clock pulses: $t_{p(clock \phi 1)}$ (See Figure 2)	0.4		10	μ s
$t_{p(clock \phi 2)}$ (See Figure 2)	0.4			μ s
Clock delay time, $t_{d(clock)}$ (See Figure 2)	0.01		10	μ s
Rise time of clock pulse, $t_r(clock)$ (See Figure 2)			5	μ s
Fall time of clock pulse, $t_f(clock)$ (See Figure 2)			5	μ s
Clock repetition rate	0		1	MHz

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at data input	-10			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at data input		-2		V
$V_{in(1)\phi}$	Input voltage required to ensure logical 1 at either clock input	-27			V
$V_{in(0)\phi}$	Input voltage required to ensure logical 0 at either clock input		-2		V
$V_{out(1)}$	Logical 1 output voltage	-11	-13		V
$V_{out(0)}$	Logical 0 output voltage	-0.3	-1		V
V_{out}	Output voltage	-10	-11		V
$I_{in(1)}$	Logical 1 level input current into data input	-6	-8		μ A
$I_{in(1)\phi}$	Logical 1 level input current into either clock input	-0.5			μ A
$I_{in(0)\phi}$	Logical 0 level input current into either clock input	-50			μ A
$z_{in\phi 2}$	Clock $\phi 2$ input impedance	38	46		k Ω
z_{out}	Output impedance	0.7	1.5		k Ω
C_{in}	Capacitance of data input	3	5		pF
$C_{in\phi}$	Capacitance of each clock input	15	18		pF
I_{DD}	Supply current into V_{DD} terminal	-7.5	-13		mA
I_{GG}	Supply current into V_{GG} terminal	-1.8	-3		mA

†Unless otherwise noted, $V_{DD} = -13$ V to -15 V, $V_{GG} = -27$ V to -29 V, $R_L = 10$ M Ω , and $C_L = 10$ pF.

‡All typical values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from clock $\phi 2$ to data output		300	450	ns
t_{pd0}	Propagation delay time to logical 0 level from clock $\phi 2$ to data output		300	450	ns

timing diagram

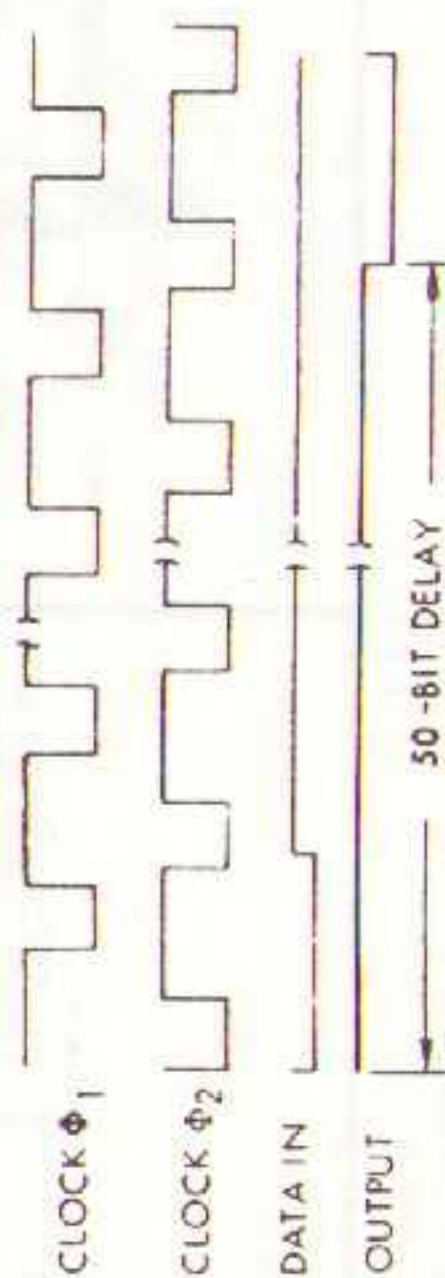


FIGURE 1

voltage waveforms

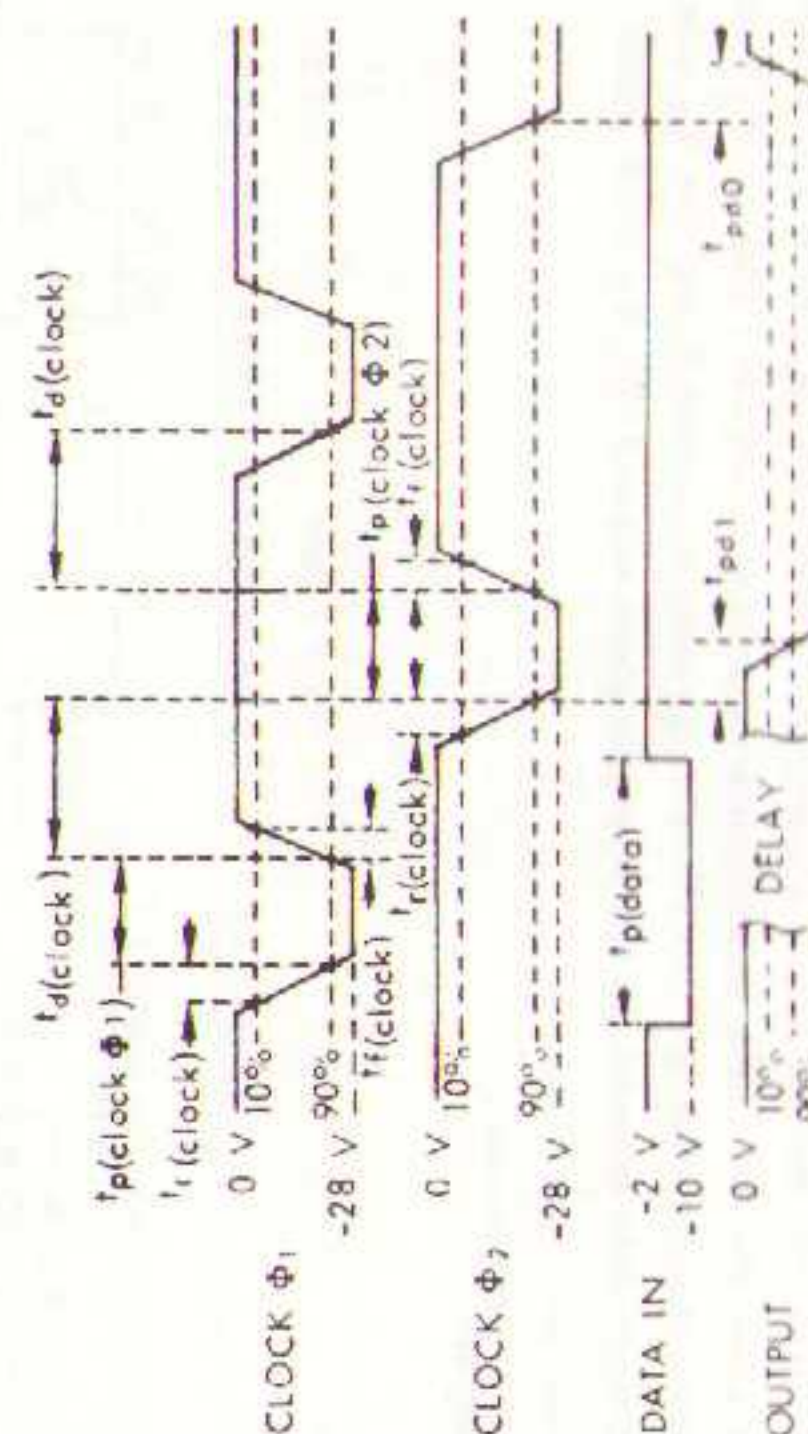


FIGURE 2

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TEXAS INSTRUMENTS

switching characteristics, $V_{DD} = -14\text{ V}$, $V_{GG} = -28\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from clock ϕ_2 to data output		300	450	ns
t_{pd0}	Propagation delay time to logical 0 level from clock ϕ_2 to data output		300	450	ns

timing diagram

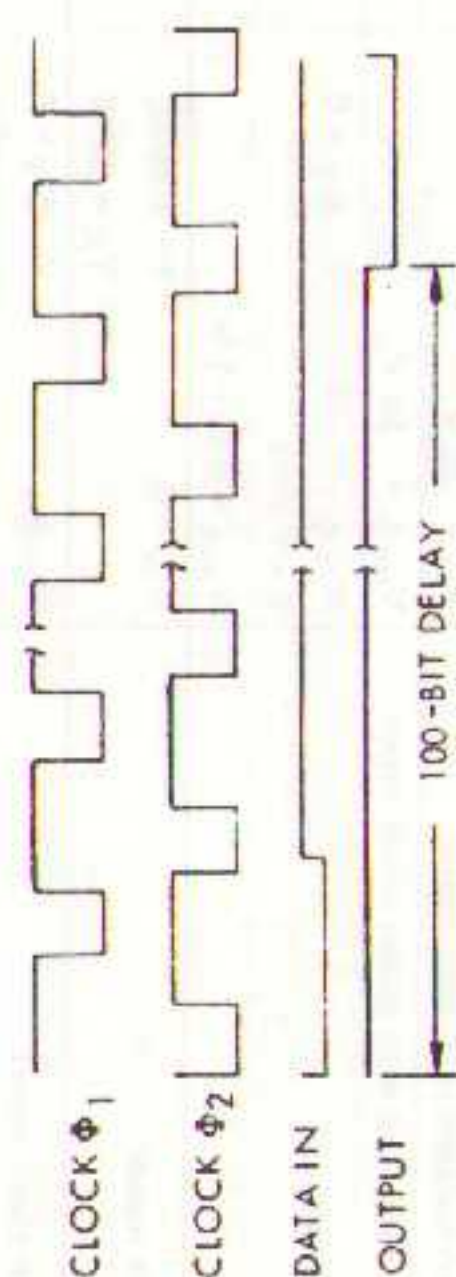


FIGURE 1

voltage waveforms

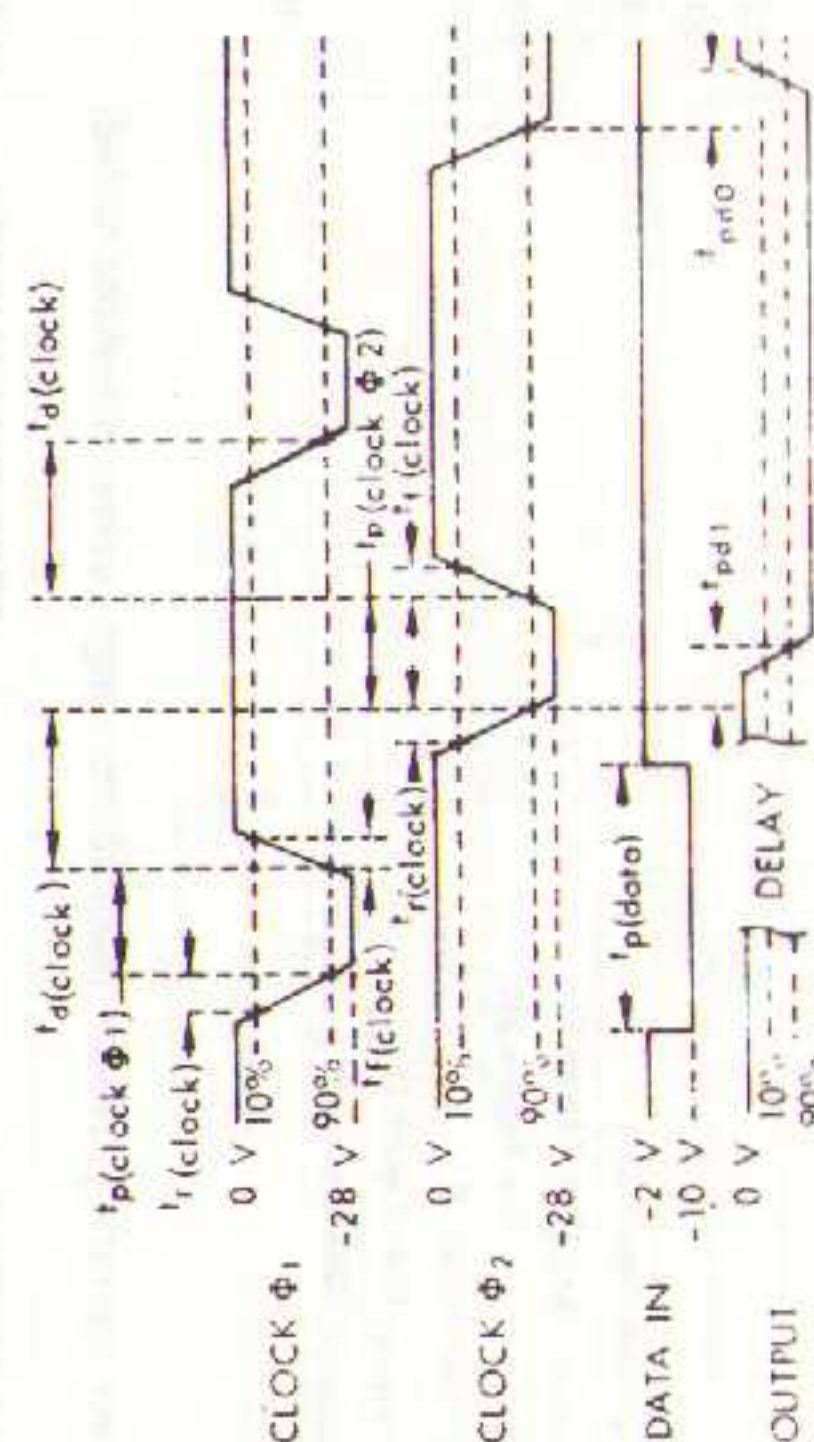


FIGURE 2

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO ADAPT THE DATA PRESENTED.

TEXAS INSTRUMENTS

Inleiding.

Coördinatie: Paul E. Annokkee

Bij het verschijnen van de eerste drie delen van de jaargang 1971 willen wij onze nieuwe abonnees op de hoogte brengen van de verschijningsdata. Onze vaste abonnees weten reeds, dat deze documentatie bestaat uit 12 delen van minimaal 20 pagina's, waarbij wij het recht voorbehouden, delen te combineren. Gezien het onregelmatig uitkomen van de verwerkte fabrieksinformaties kan deze technische documentatie niet als maandblad worden gekenmerkt. Wij verzekeren U echter, dat als U eenmaal in ons adresseersysteem bent opgenomen en eventuele adreswijzigingen op tijd aan ons doorgeeft, U verzekerd kunt zijn van toezending dezer documentatie.

Mocht U over uw abonnement o.i.d. willen corresponderen, vergeet U dan niet Uw abonneenummer te vermelden? Ons adres is:

N.V. Technische Handelmaatschappij Van Dam Elektronica, Postbus 3149 te Rotterdam-noord, Holland.

Characteristics and Applications of the SN7413N Dual Schmitt Trigger



Application Report B81

By Bob Parsons

When high-speed logic gates are driven directly by input signals with slow rise and fall times, it is possible for the gates to produce false outputs (Figure 1). Oscillation occurs when the input signal is held in the linear region of the V_{in} - V_{out} characteristic (Figure 2) for a period equal to or greater than the sum of the gate propagation delays ($t_{PHL} + t_{PLH}$). When this occurs the gate behaves as a linear amplifier with high gain and the various feedback paths (Figure 3) contribute to instability and consequent false outputs.

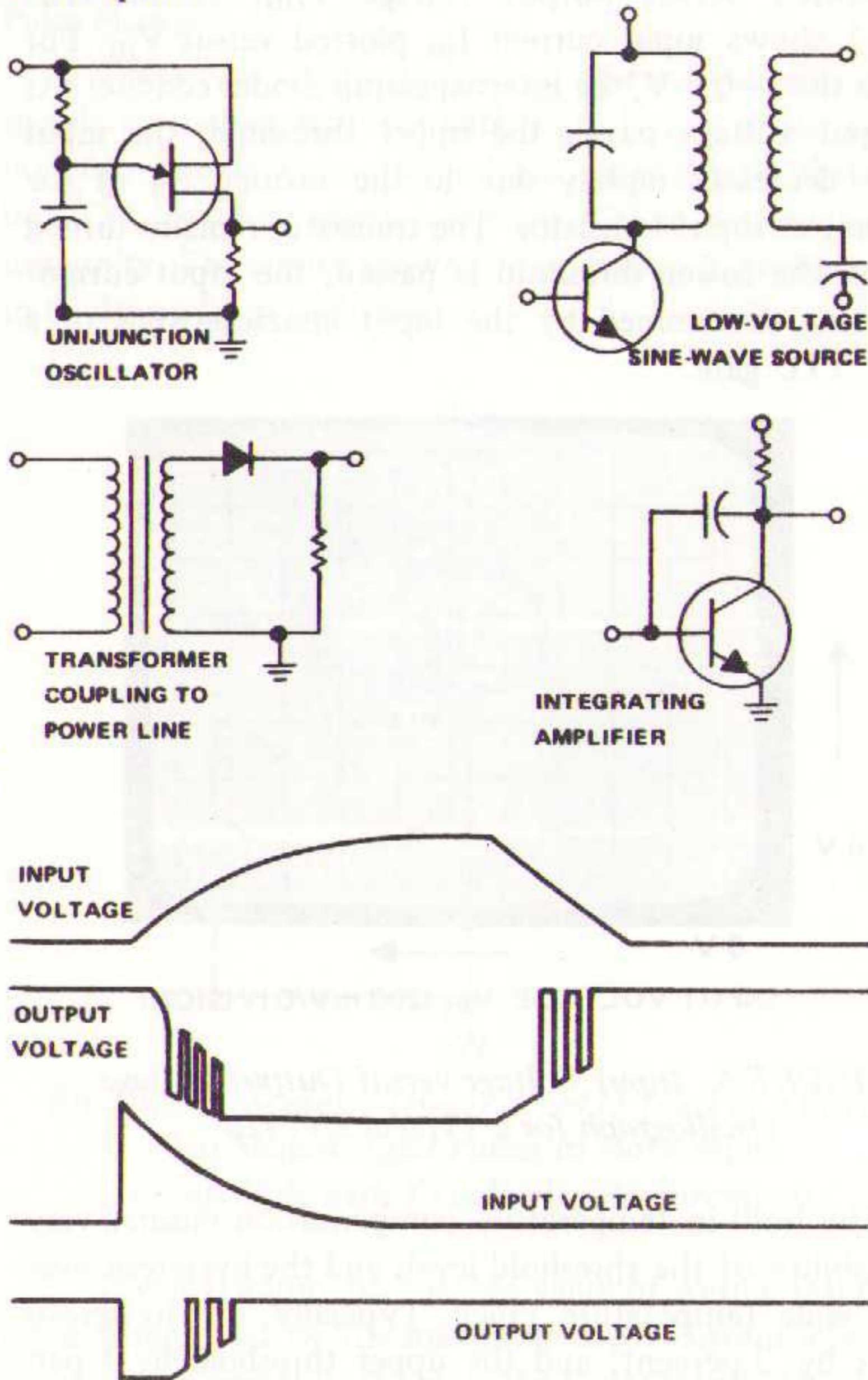


FIGURE 1. Generators of Slow Rise and Fall Time Signals. Reaction of a high-speed logic gate to these signals

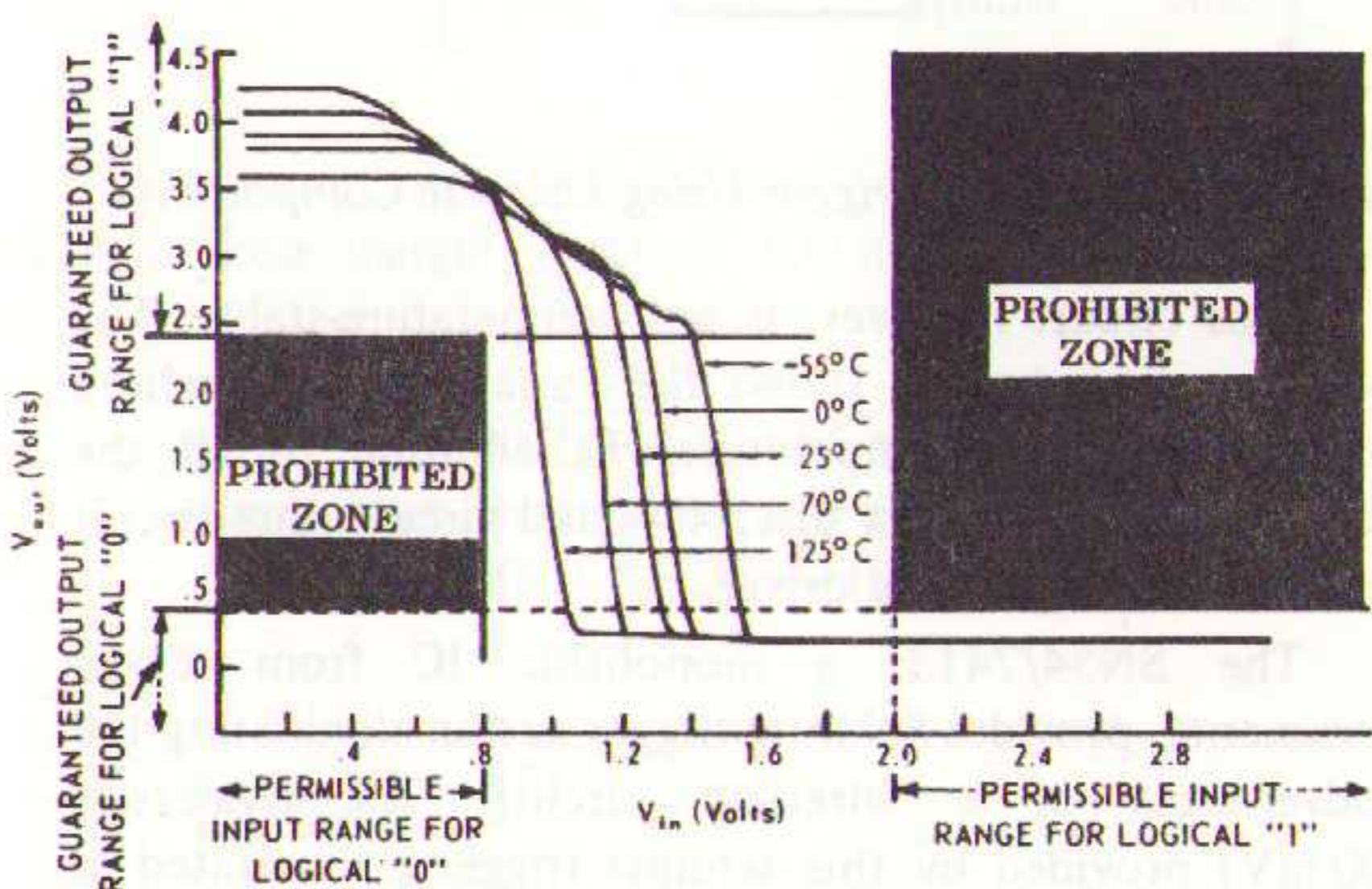


FIGURE 2. Typical Transfer Characteristics for SN54/7400 Gates

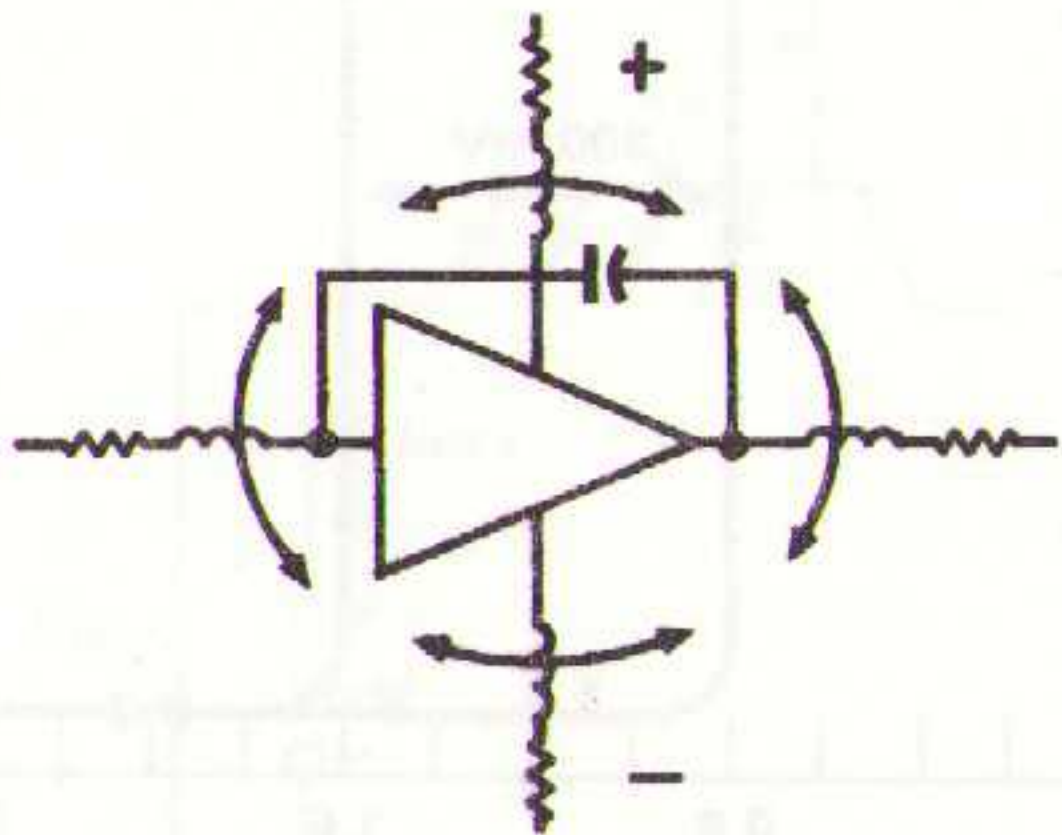
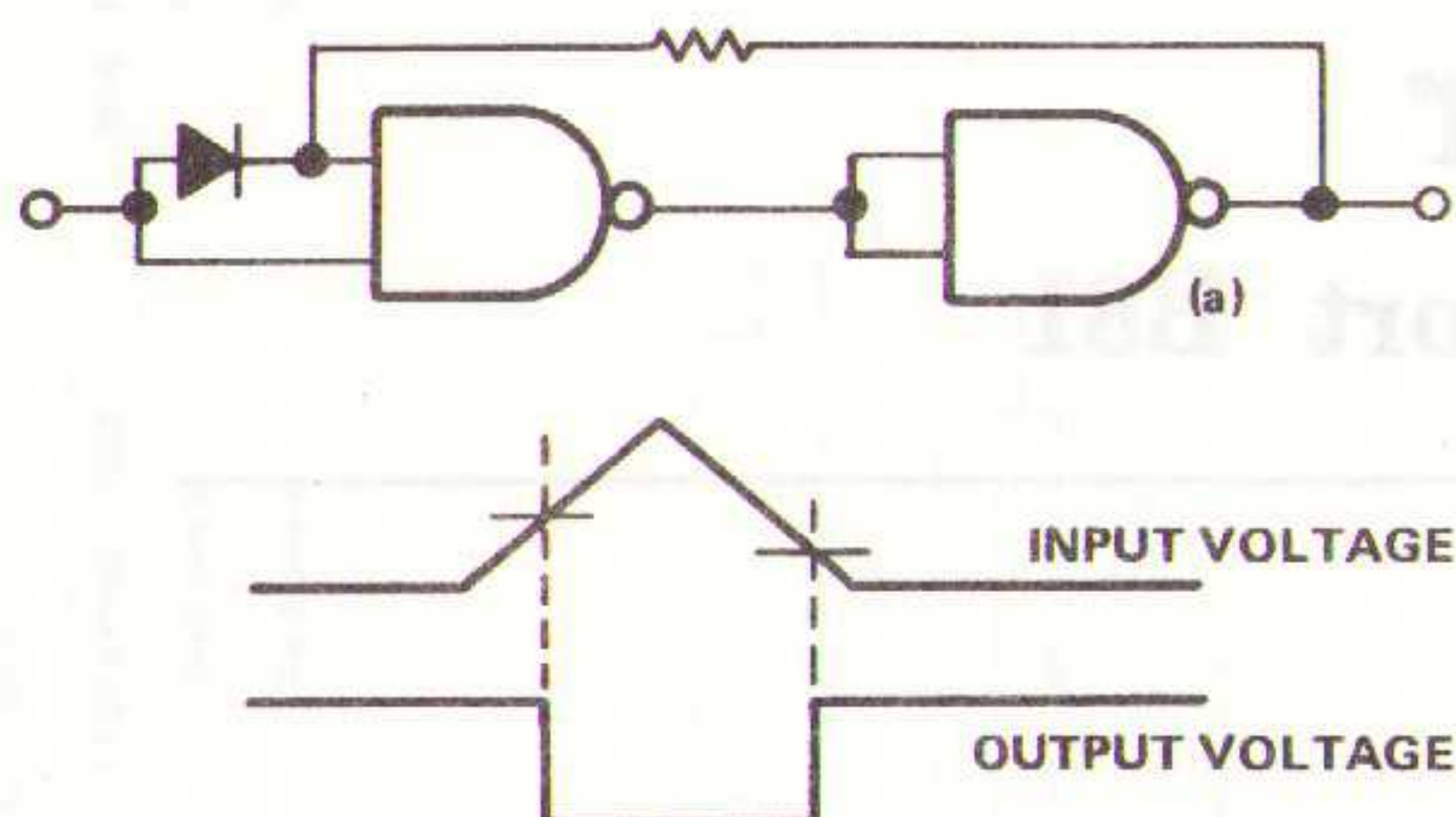


FIGURE 3. Gate Behaving as Linear Amplifier with Possible Feedback Paths

One solution to slow-rise-time problems is the introduction of hysteresis in the V_{in} - V_{out} characteristic with a discrete Schmitt trigger arrangement shown in Figure 4. The Schmitt trigger's positive feedback introduces a snap action that eliminates oscillation. Another advantage of this hysteresis is the increased d-c noise margin. D-c noise margin is defined as the difference between the guaranteed logic-state voltage limits of a driving gate and the voltage requirements of a driven device.

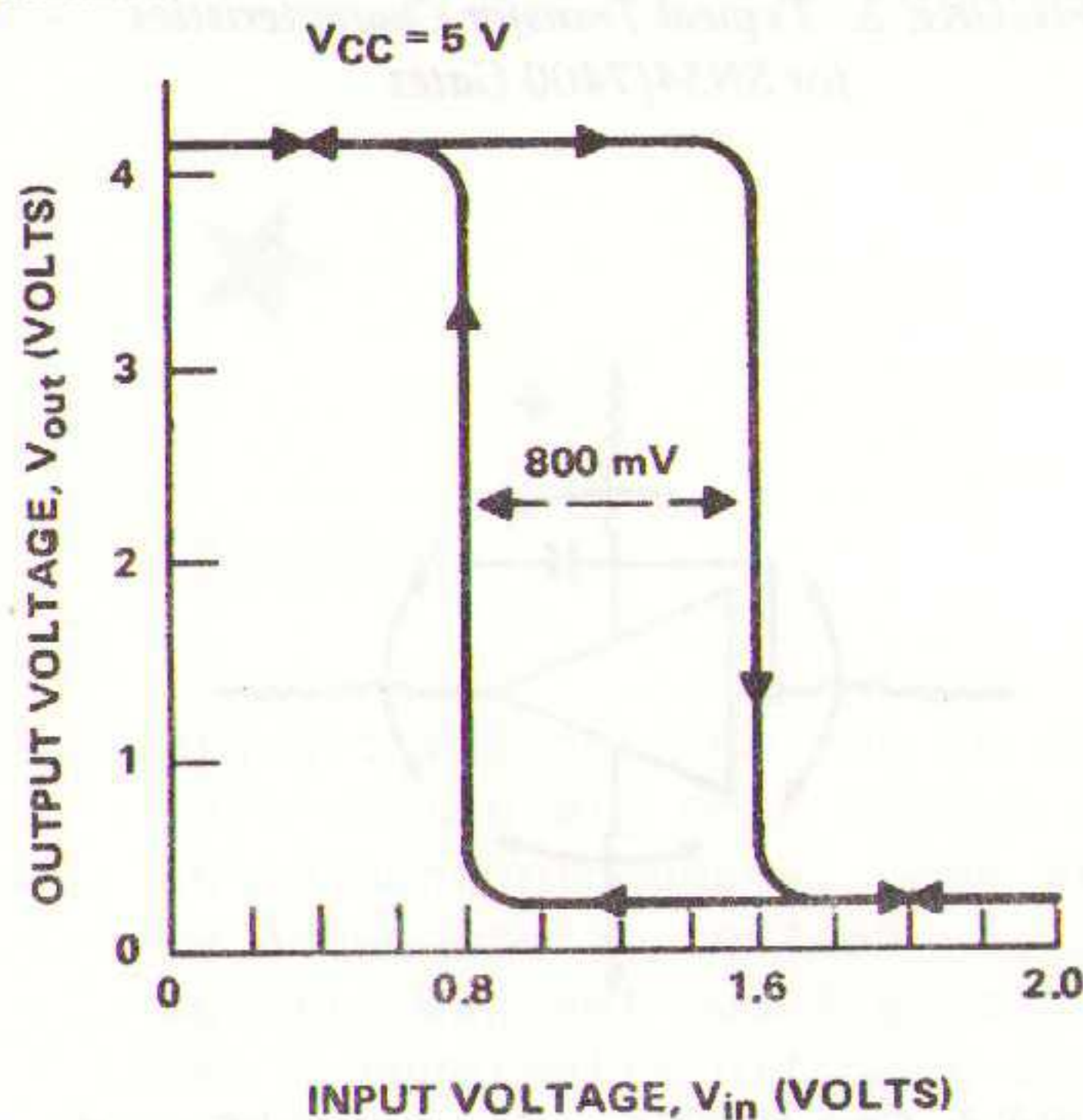


CA27173

FIGURE 4. Schmitt Trigger Using Discrete Components

This circuit however, is not temperature-stable. The V_{in} - V_{out} characteristic shows the variations of threshold voltage levels with temperature. In addition to all the disadvantages of being a discrete-wired circuit, this circuit requires a low-impedance driver.

The SN54/7413, a monolithic IC from Texas Instruments, provides Schmitt trigger action eliminating the disadvantages of a wired-up circuit. The hysteresis (800 mV) provided by this schmitt trigger is illustrated in Figure 5. In addition the SN54/7413 is temperature-compensated.



CA27174

FIGURE 5. V_{in} - V_{out} Characteristic of SN7413 Showing Hysteresis

For convenience this report discusses only the SN7413. However all statements made about the SN7413 are also true of the SN5413 which is distinguished by being characterized in the military temperature range.

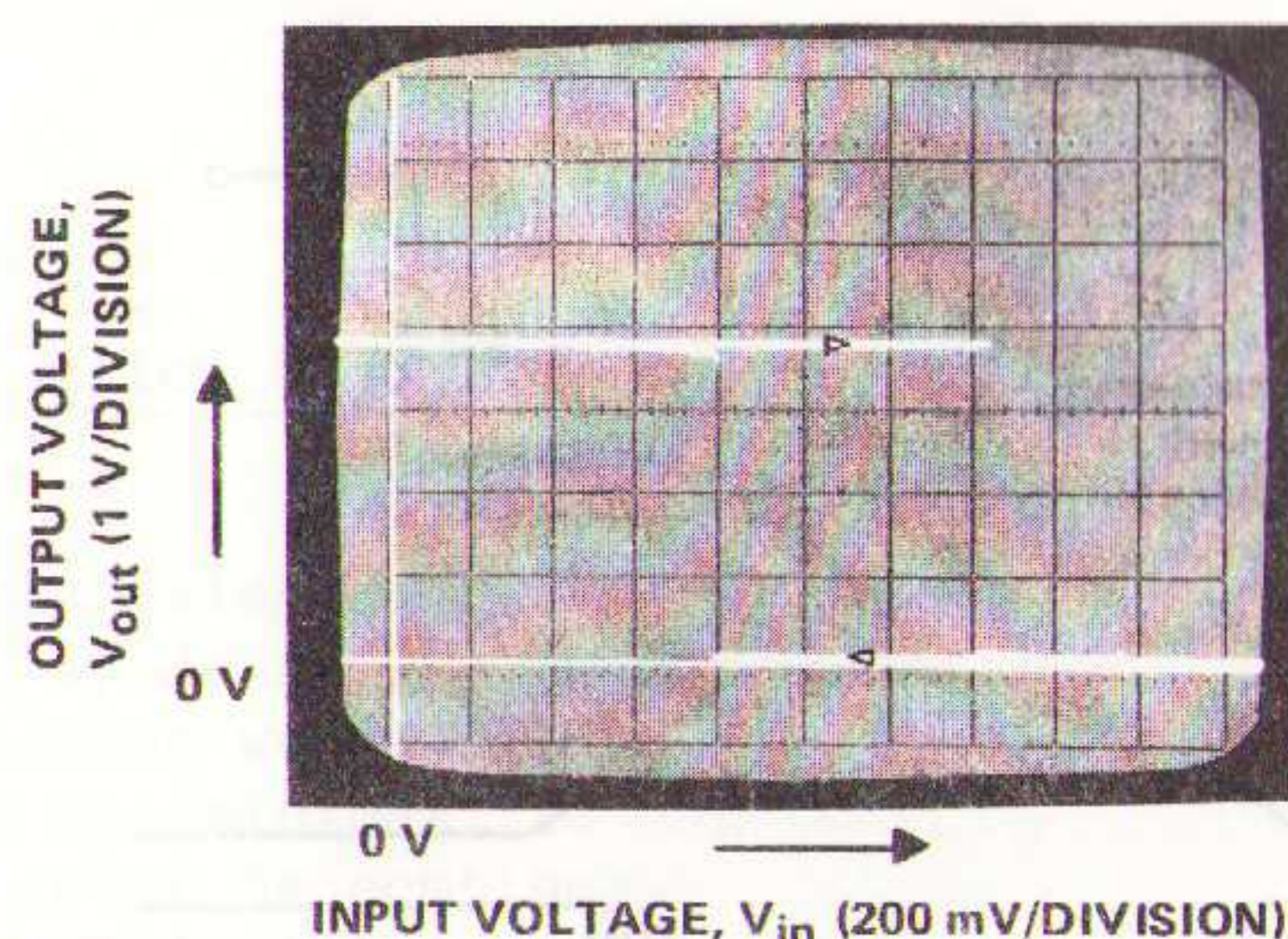
Data specifications of the SN7413 are not included in this report but are available on request.

SN7413 CHARACTERISTICS

The SN7413 dual Schmitt trigger consists of two identical Schmitt trigger circuits in monolithic integrated circuit form. The internal circuitry does not resemble Figure 4 but has simpler faster arrangement. Logically, each circuit functions as a 4-input NAND gate, but because of the Schmitt action the gate has different input-threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800 mV (see Figure 5).

The SN7413 is fully compatible with many TTL families because it has a totem-pole output section and multiemitter-transistor inputs clamped by diodes to the substrate. The logical 1 and 0 output levels (referred to in the data sheet as "high" and "low" respectively) are identical to those of standard TTL. The propagation delay from input to output is typically 16 ns.

Figures 6 and 7 show the input-output voltage characteristics of the SN7413. Figure 6 shows input voltage V_{in} plotted versus output voltage V_{out} at 100 kHz. Figure 7 shows input current I_{in} plotted versus V_{in} . For V_{in} less than -0.5 V, the internal clamp diodes conduct. As the input voltage passes the upper threshold, the input current decreases rapidly due to the turning off of the multiemitter input-transistor. The transistor remains turned off until the lower threshold is passed, the input current then being determined by the input characteristics of a normal TTL gate.



CA27175

FIGURE 6. Input Voltage versus Output Voltage Oscilloscope for a Typical SN7413

The built-in temperature compensation ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3 percent, and the upper threshold by 1 percent, over the temperature range of -55°C to 125°C. The SN7413 can be triggered from the slowest of input ramps and still give a clean, jitter-free output signal. It can also be triggered from straight d-c levels.

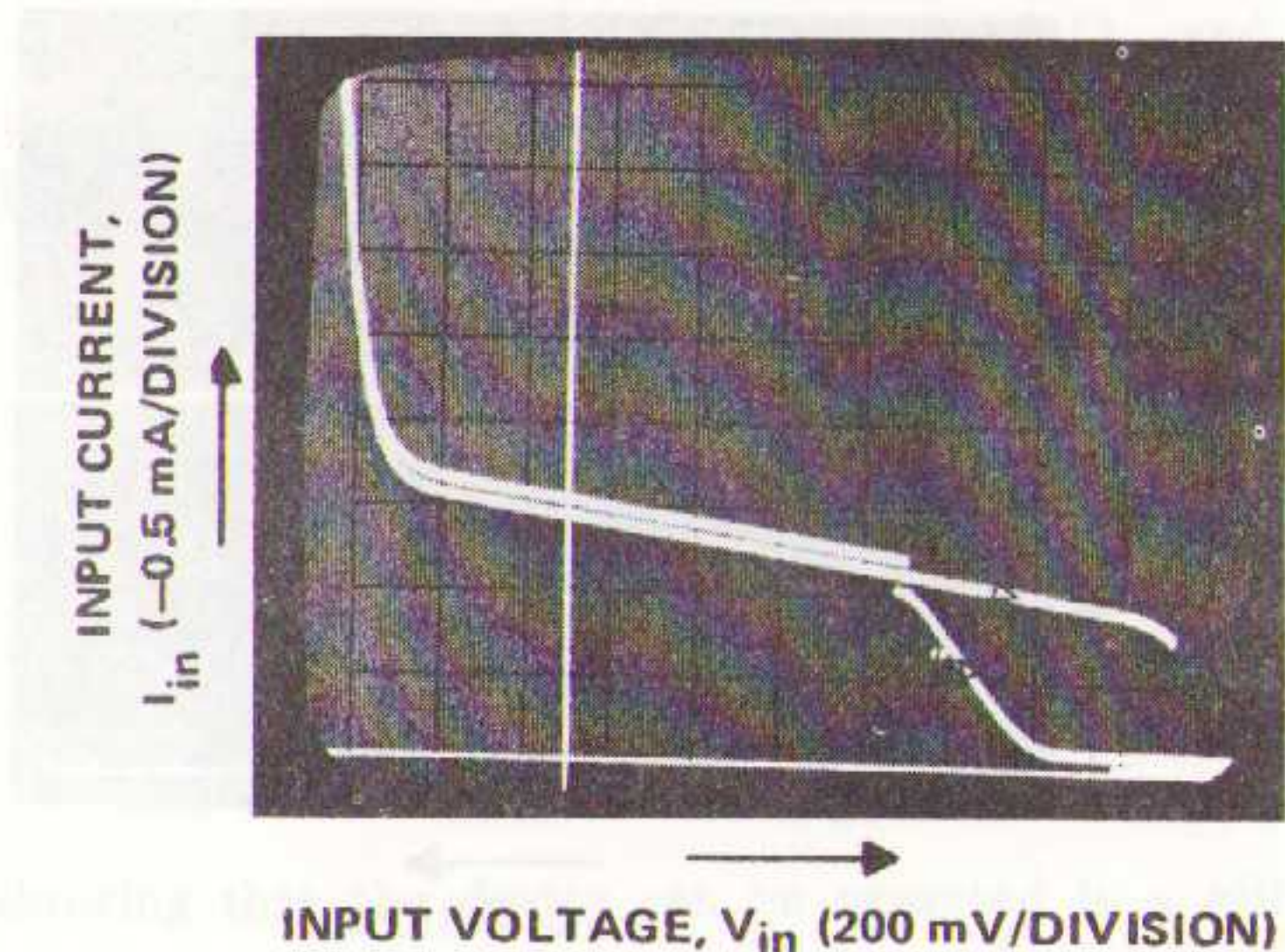


FIGURE 7. Input Voltage versus Input Current Oscillograph for SN7413

APPLICATIONS

One of the most direct applications of the Schmitt trigger is as a pulse-shaper interface between slow rise and fall input signals and a fast TTL gate.

Pulse Shaper

There are many instances where available input signals are not compatible with TTL. For example, a data waveform might have rise and fall times greater than $1\mu s$, but TTL requires edges less than 50 ns for good noise immunity. The circuit shown below, Figure 8, enables TTL to be driven from such sources.

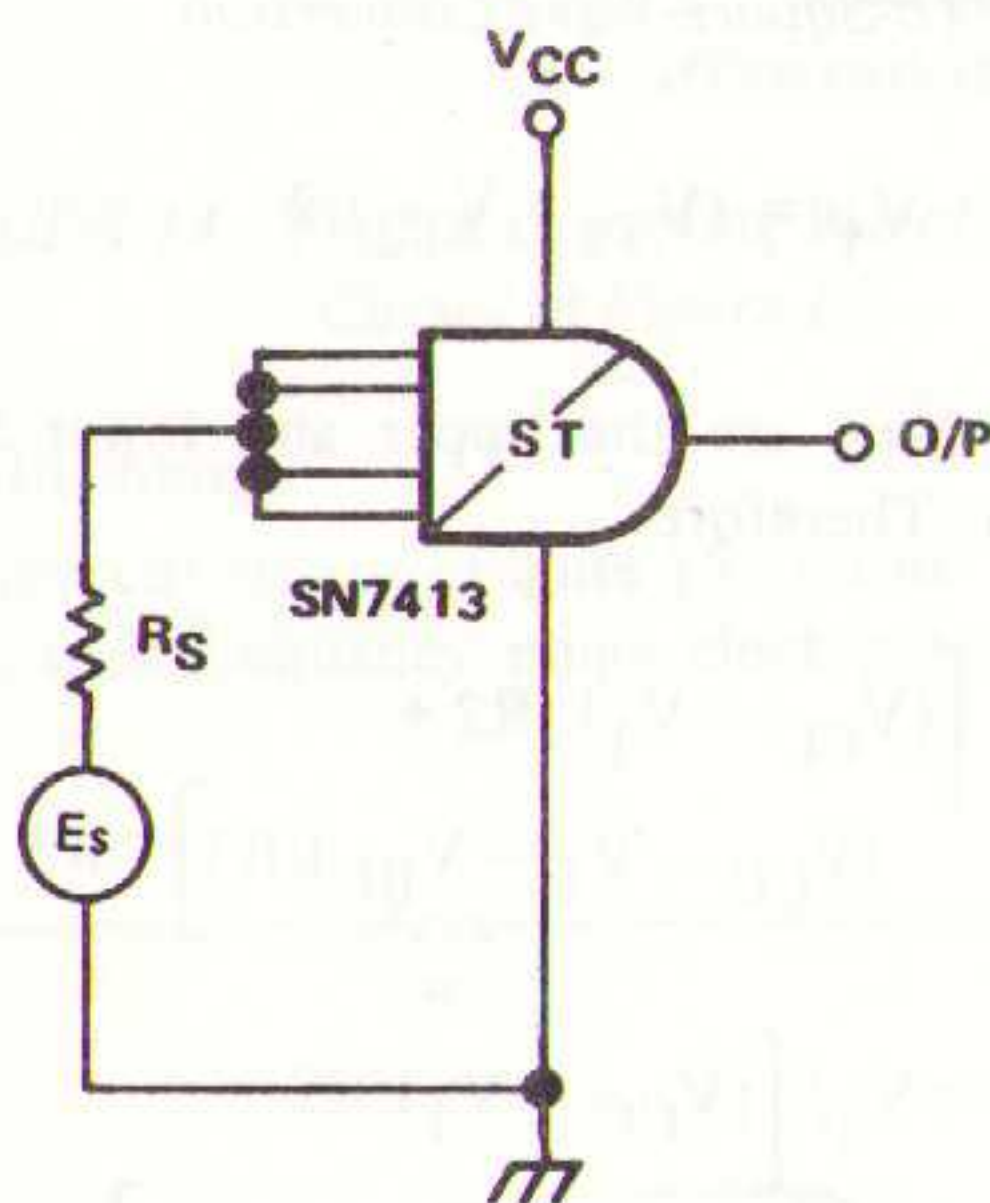


FIGURE 8. Schmitt Trigger SN7413 Used in a Circuit That Shapes Input Pulses to Make them Compatible with TTL Device Requirements

The maximum permissible value of source resistance R_S is determined by the maximum input current when the input is at a logical 0, or below the lower threshold voltage. To ensure a noise margin of 1100 mV, the input current is measured when V_{in} equals 400 mV. A maximum I_{in} of 1.6 mA at $V_{in} = 0.4$ V is guaranteed on the data sheet. Therefore $R_{S(max)} = V_{in}/I_{in(max)} = 400/1.6 = 250 \Omega$. For noise margins other than 1100 mV, or $V_{in} = 0.4$ V, the

minimum value of internal base resistor R_1 must be deducted from data-sheet guarantees in order to determine a maximum value of resistor R_S . Figure 9 illustrates the variables determining the value of resistor R_1 . For $V_{in} = 0.4$ V, $V_{CC(max)} = 5.25$ V, $R_{1min} = [V_{CC(max)} - V_{BE}]/I_{max}$, $R_{1min} = (5.25 - 0.75)/1.6$, $R_{1min} = 2.56$ k Ω . For a noise margin V_{NM} , the maximum value of resistor R_S in Figure 10 is given by

$$R_{S(max)} = \frac{(V_{T(min)} - V_{NM}) R_1}{[(V_{CC} - V_{BE}) - (V_{T(min)} - V_{NM})]}$$

For a noise margin V_{NM} of 100 mV and $V_{CC} = 5.0$ V

$$R_{S(max)} = \frac{(0.7 - 0.1) 2.56 \times 10^3}{(5.0 - 0.75) - (0.7 - 0.1)}$$

$$R_{S(max)} = 421 \Omega$$

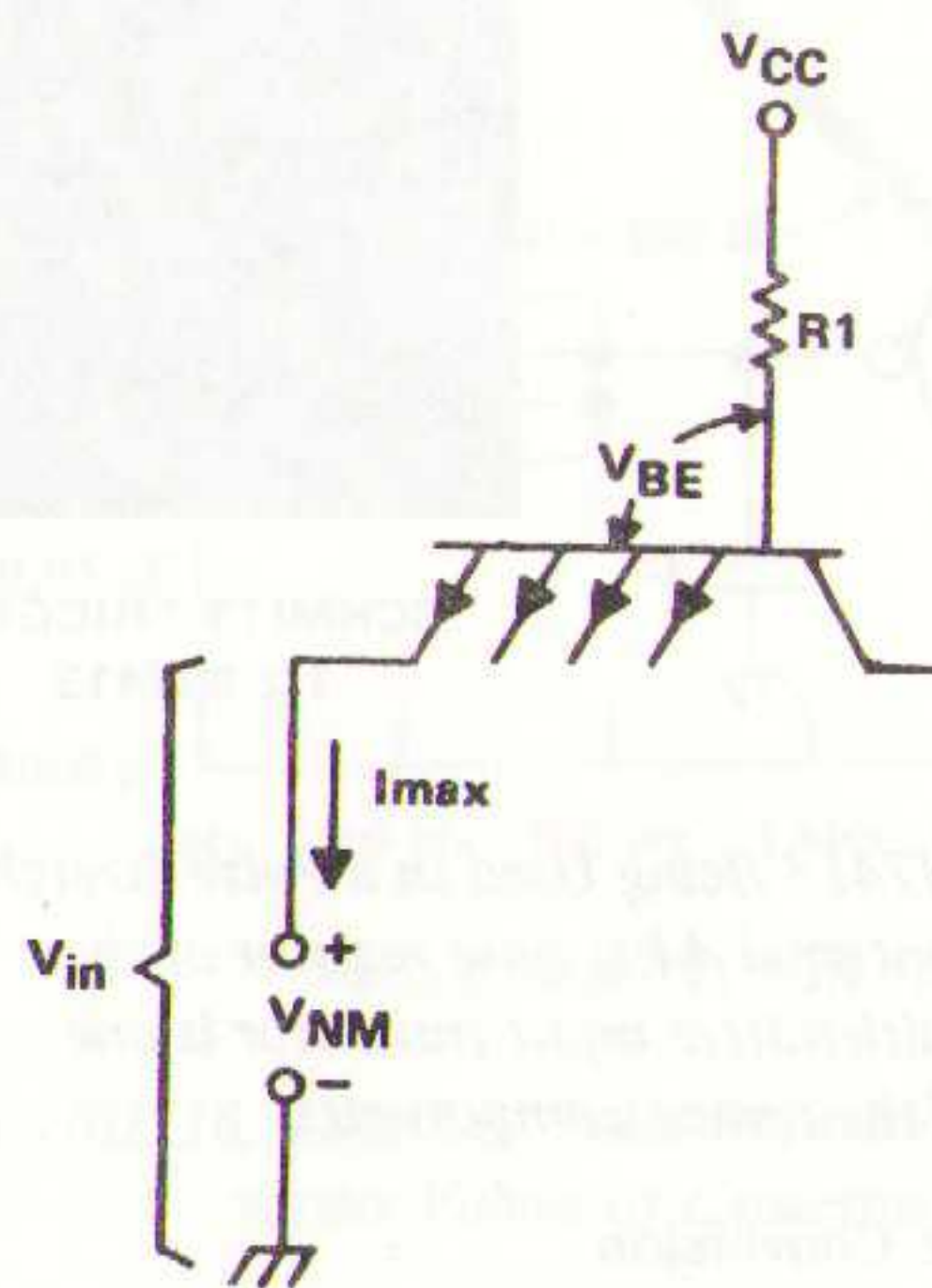
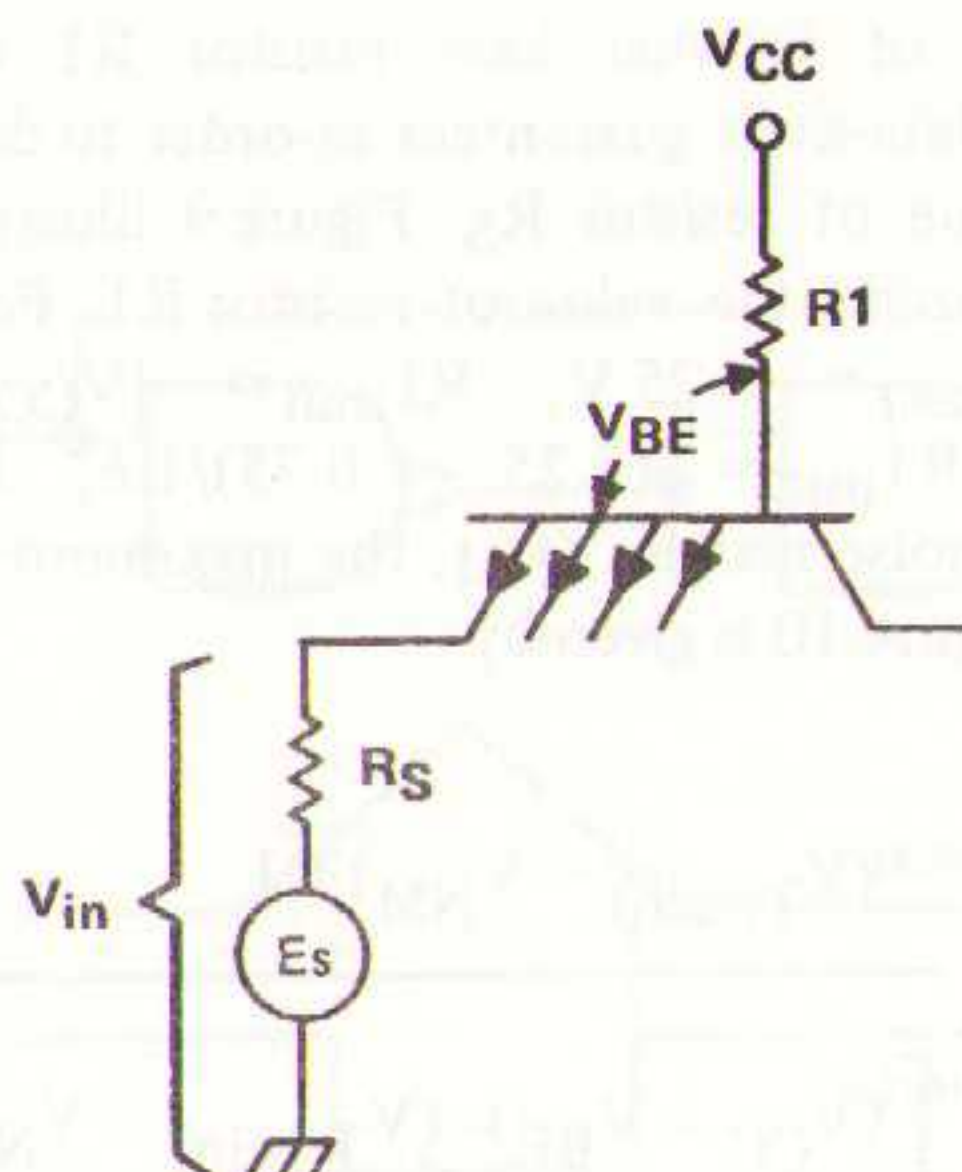


FIGURE 9. Variables That Determine the Minimum Value of Internal Base Resistor R_1

Pulse Stretcher

This circuit (Figure 11) uses the internal 4-k Ω base resistor of the Schmitt multiemitter input transistor as one of the timing components.

There is a small delay between the leading edges of the input and output pulses; due to the time taken to discharge capacitor C through the saturation resistance of the output transistor of the SN7401.

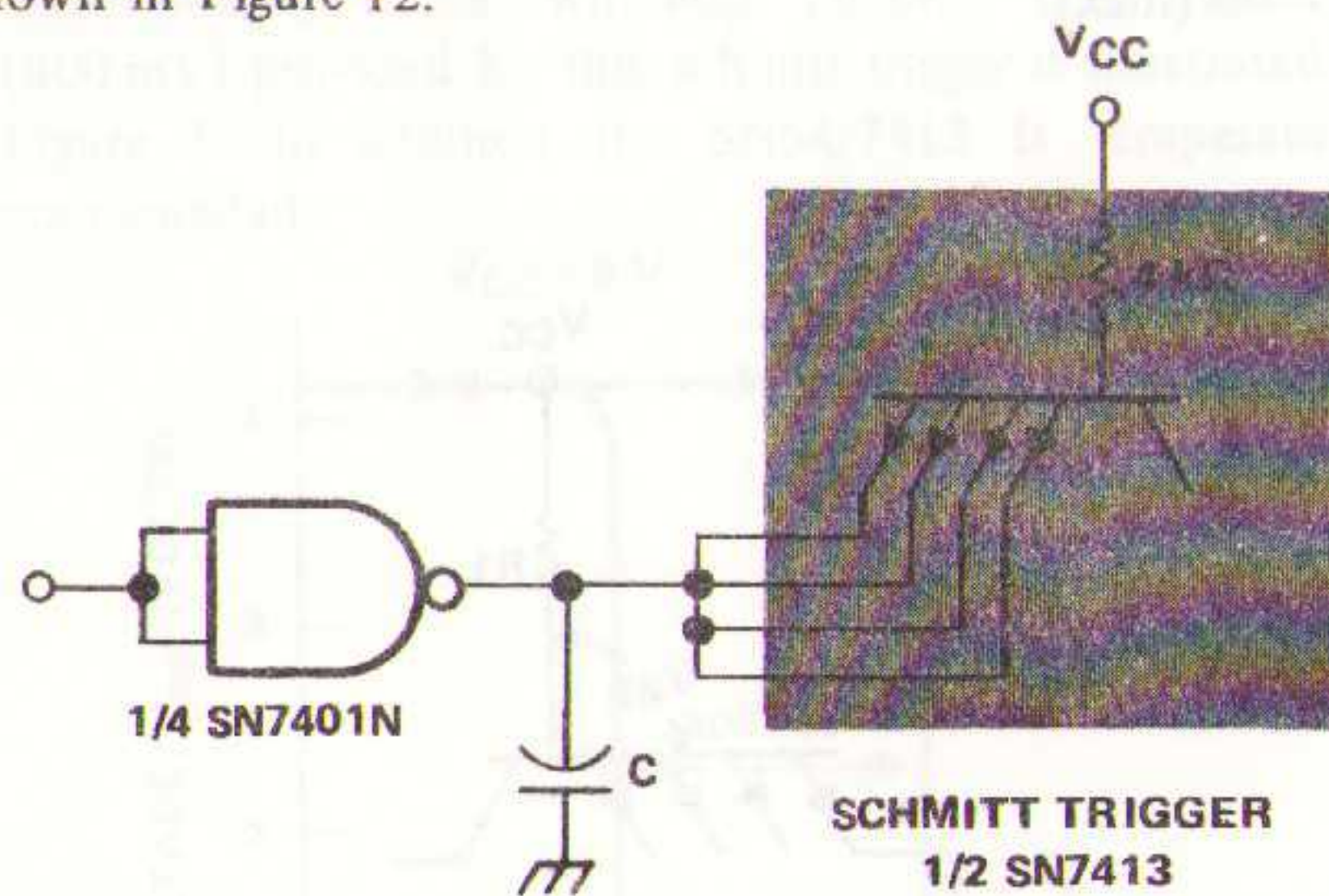


CA27181

FIGURE 10. Variables Used in the Determination of the Maximum Value of R_S for a Given Noise Margin

For high repetition rates and large values of capacitor C , the mean dissipation in the SN7401 output stage should be limited to 60 mW or 35 mA peak current or 16 mA steady-state by inclusion of a series resistor between its output and capacitor C .

Typical operating waveforms for this circuit are shown in Figure 12.



CA27182

FIGURE 11. SN7413 Being Used in a Pulse-Stretcher Circuit. The internal $4\text{-k}\Omega$ base resistor of the Schmitt multiemitter input transistor is one of the timing components

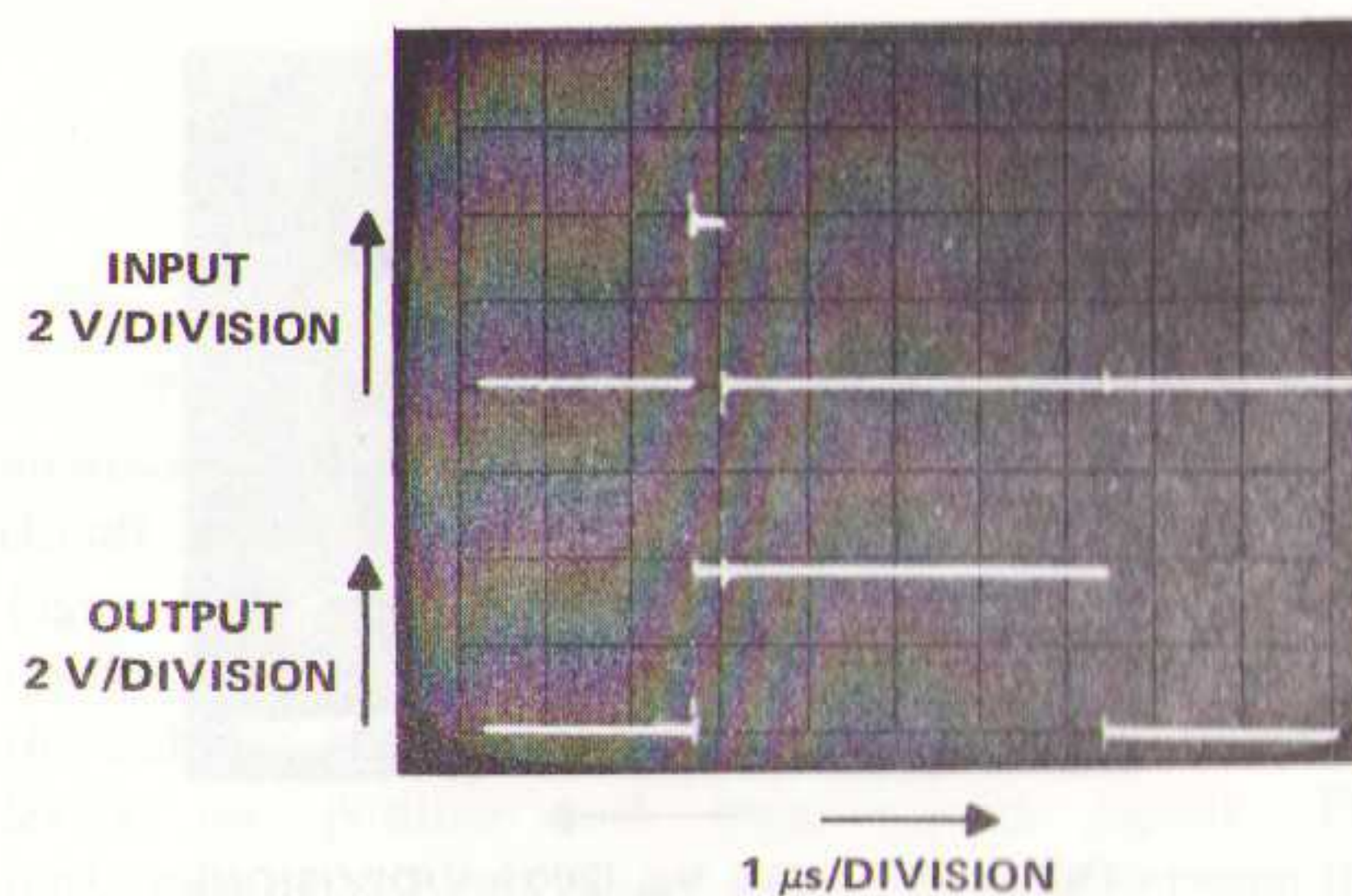
Sine-to-Square-Wave Conversion

Sine-to-square-wave conversion, one of the simplest applications of the Schmitt Trigger, is illustrated in Figure 13.

The resistive divider R_2 and R_3 biases the Schmitt trigger input midway between the upper and lower thresholds. This gives a 50 percent duty cycle with sinusoidal inputs. The values of resistors R_2 and R_3 may be determined as follows:

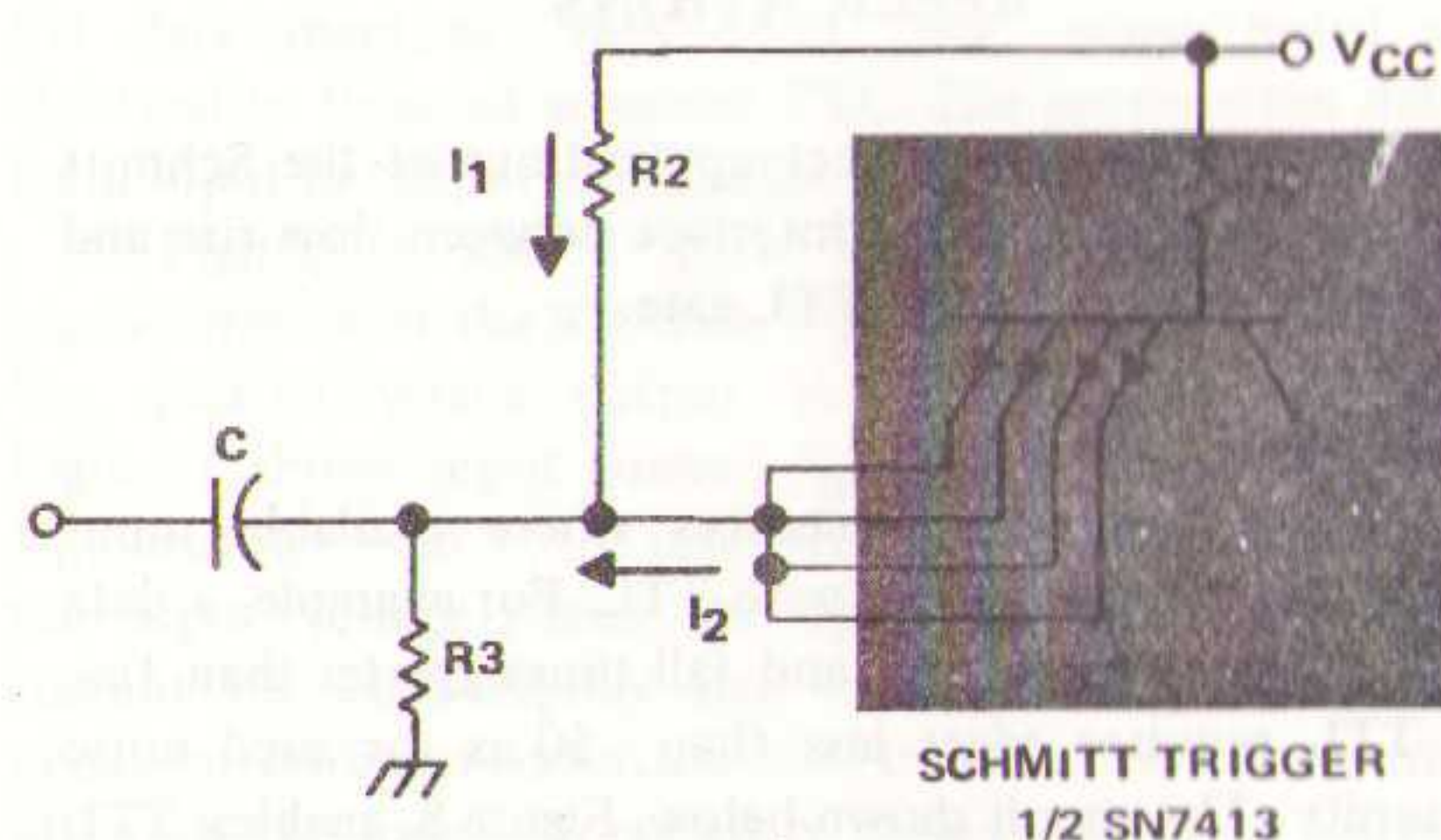
The voltage at the multiemitter input is given by

$$V_1 = (I_1 + I_2) R_3$$



CA27183

FIGURE 12. Typical Operating Waveforms for Pulse Stretcher Circuit in Figure 11



CA27177

FIGURE 13. SN7413 Used in a Circuit for Sine-To-Square-Wave Conversion

but

$$V_1 = (V_{T1} + V_{T2})/2$$

where V_{T1} and V_{T2} are the upper and lower Schmitt trigger thresholds. Therefore

$$V_1 = \left[\frac{(V_{CC} - V_1)/R_2 + (V_{CC} - V_1 - V_{BE})/R_1}{R_3} \right] R_3$$

or

$$R_3 = V_1 / \left[\frac{(V_{CC} - V_1)/R_2 + (V_{CC} - V_1 - V_{BE})/R_1}{R_3} \right] \quad (1)$$

and

$$R_2 = \frac{(V_{CC} - V_1) R_3 R_1}{[R_1 V_1 - R_3 (V_{CC} - V_{BE} - V_1)]} \quad (2)$$

Typical values for the variables in Equations (1) and (2) are $V_{T1} = 1.7\text{ V}$, $V_{T2} = 0.9\text{ V}$, $V_{CC} = 5.0\text{ V}$, $R_1 = 4.0\text{ k}\Omega$, and $V_{BE} = 0.75\text{ V}$.

Thus choosing resistor $R_3 = 470\ \Omega$, and substituting in Equation (2), we have $R_2 = 1.83\ \text{k}\Omega$; that is $R_3 = 470\ \Omega$ and $R_2 = 1.8\ \text{k}\Omega$ in preferred values.

If $R_2 = \infty$ then Equation (1) becomes

$$R_3 = \frac{R_1}{\left[2 \left[\frac{(V_{CC} - V_{BE})}{(V_{T1} + V_{T2})} \right] - 1 \right]}$$

Substituting values in this equation gives

$$R_3 = 1.76\ \text{k}\Omega \text{ or } 1.8\ \text{k}\Omega$$

showing that the device can be operated in a self biased mode.

The circuit of Figure 13 is suitable for use up to 8 MHz with sinusoidal inputs. The value of capacitor C should be such that its reactance at the operating frequency is very much less than $R_2 R_3 / (R_2 + R_3)$.

Typical operating waveforms obtained with the self-biased mode at 1 MHz are shown in Figure 14.

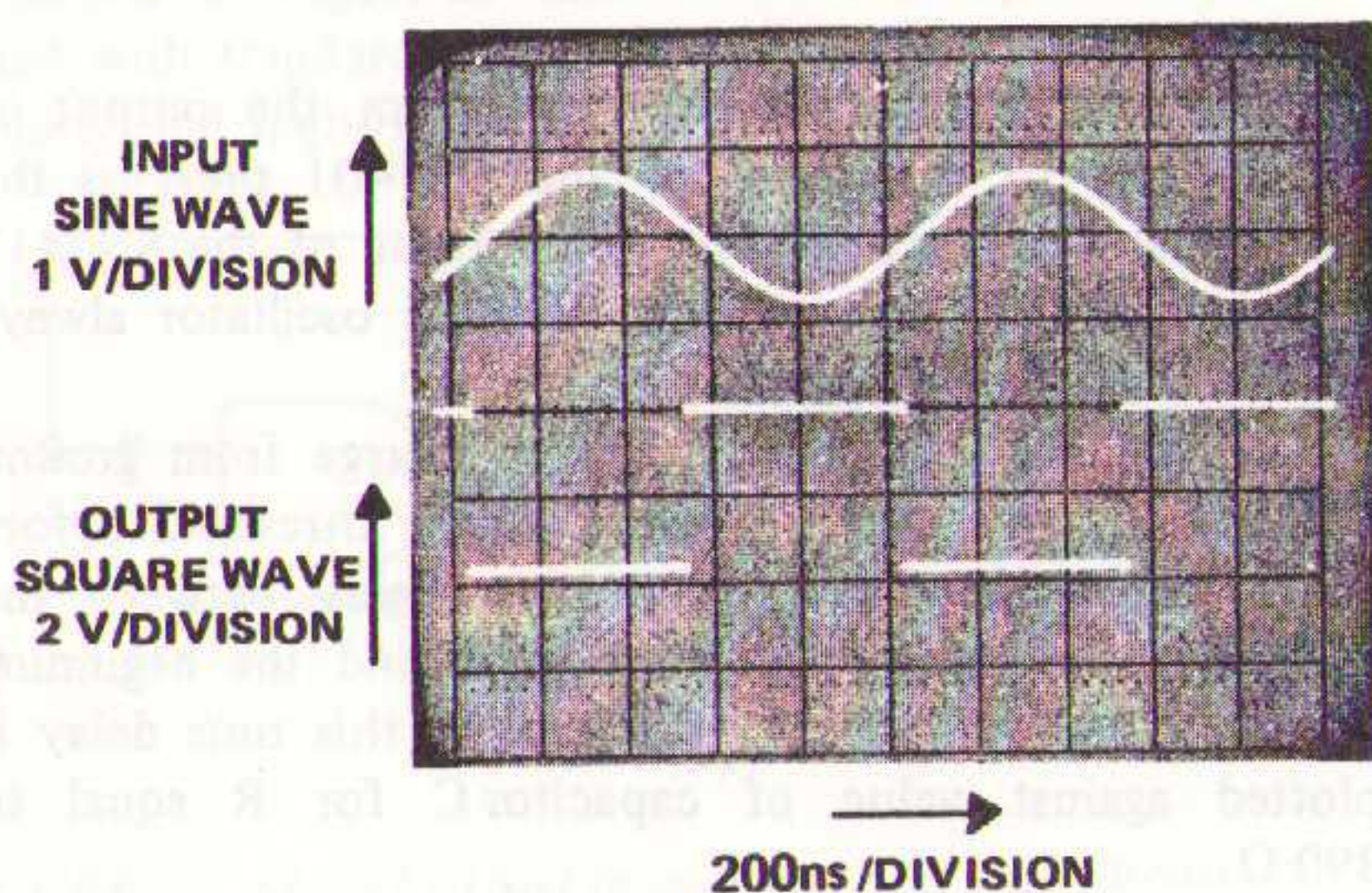


FIGURE 14. Typical Operating Waveforms for the Circuit in Figure 13

R-C Multivibrator

The circuit of Figure 15 forms the basis of a versatile wide-frequency range clock-pulse source.

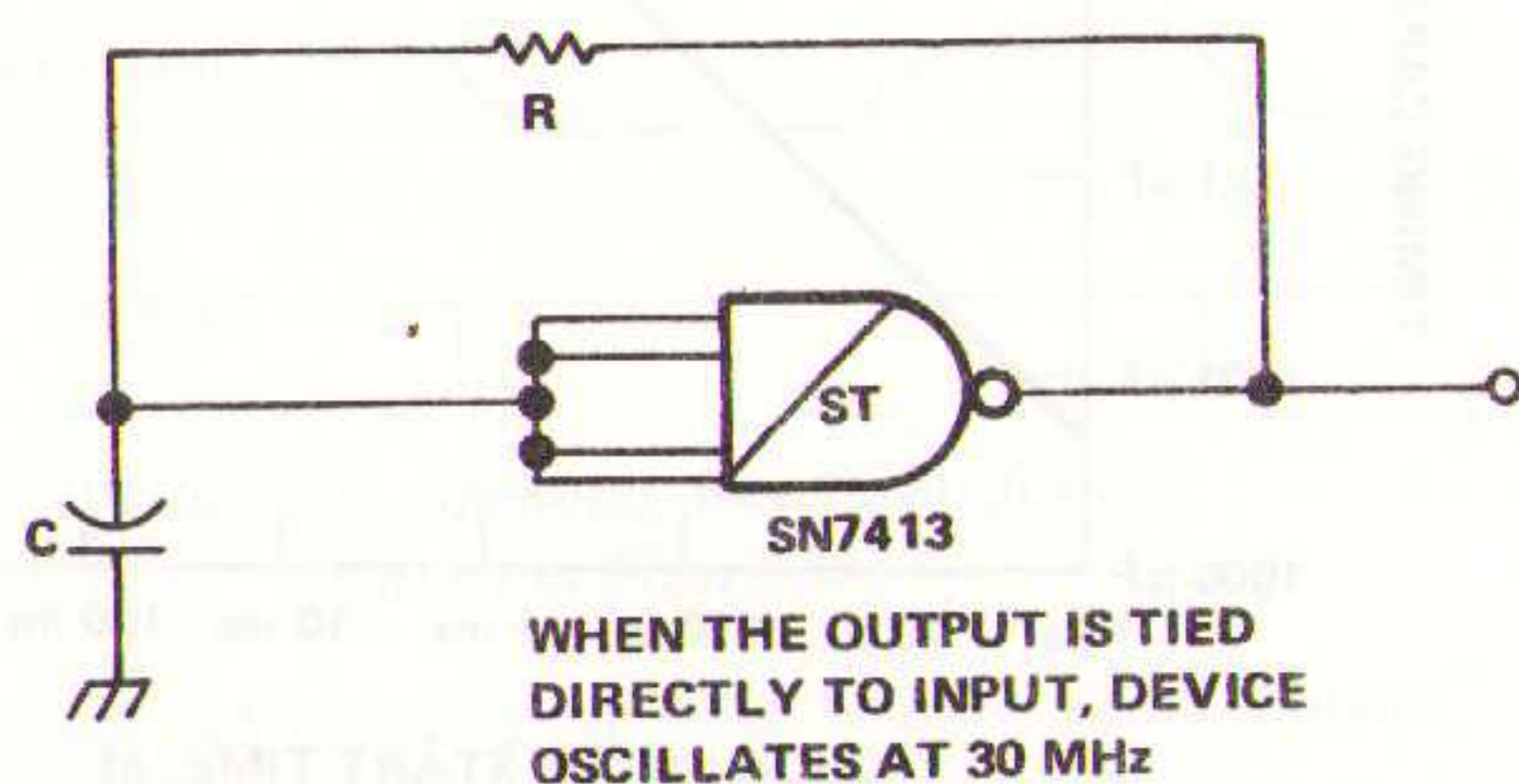


FIGURE 15. SN7413 Used in a R-C Multivibrator. This circuit forms the basis of a versatile wide-frequency range clock-pulse source

The circuit is self-starting and a frequency range of 8 decades is possible by changing the value of capacitor C . Circuit operation is as follows: Initially capacitor C is discharged and the Schmitt output is at a logical 1. Capacitor C then charges towards $(V_{CC} - V_{BE} - V_F)$ through resistor R , until the upper threshold voltage is reached. The output then changes to a logical 0 and capacitor C discharges to the lower threshold voltage through resistor R . The cycle then repeats.

The limiting values of resistor R are determined by the voltage dropped across it when the input is approaching the lower threshold and the output is at a logical 0. The lower value is determined by the output impedance of the Schmitt trigger in the logical 1 state. The output voltage should be sufficient to ensure a logical 1 at the input of succeeding stages when the input to the Schmitt trigger is at the lower threshold voltage. The calculation of the resistor's optimum value for a given load is lengthy and only results of this calculation will be stated here. For a fan-out of 2 over the full temperature range, resistor R should be $390\ \Omega$.

Figure 16 is a graph of pulse-repetition frequency versus values of capacitor C .

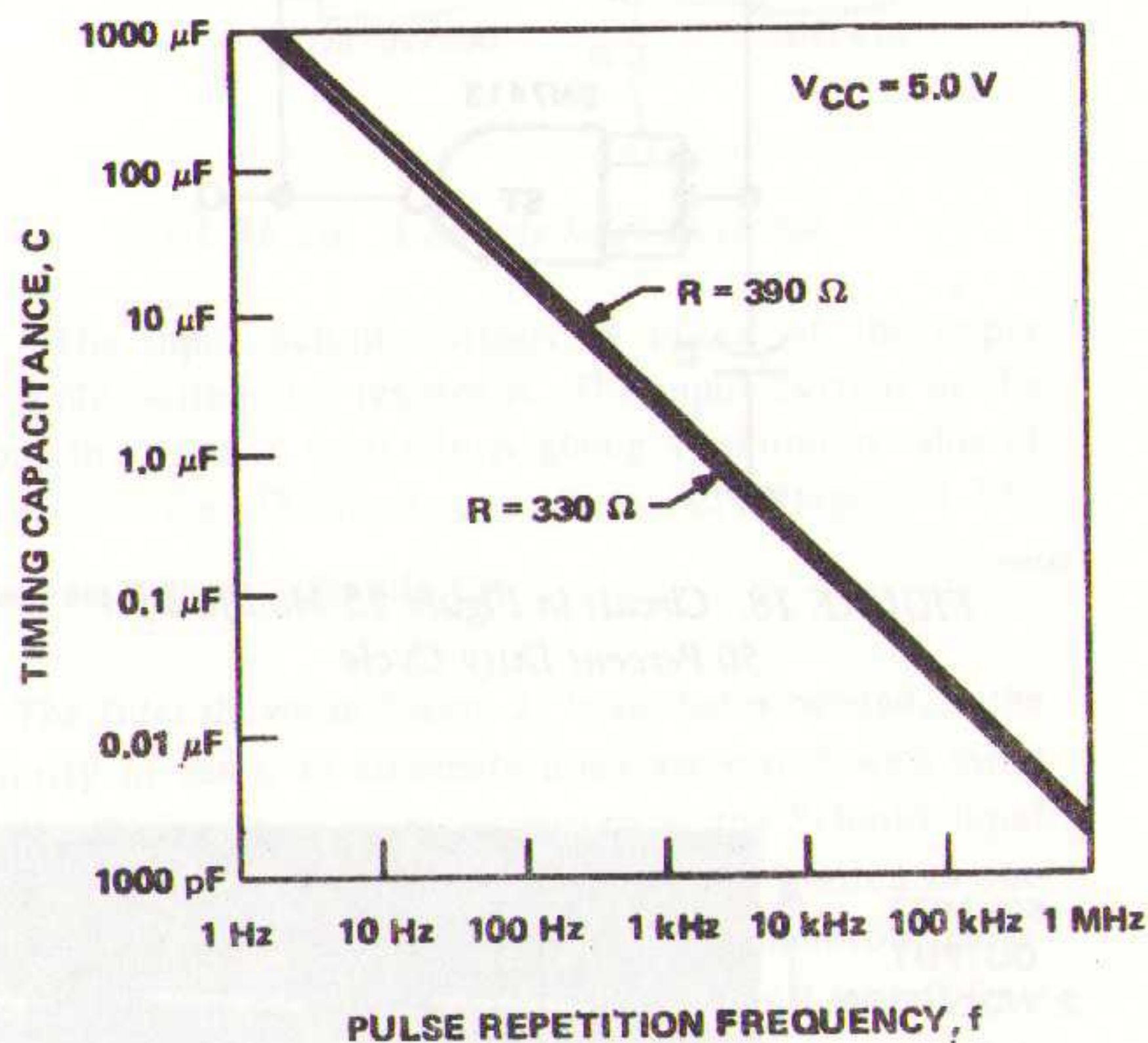


FIGURE 16. Graph of Pulse-Repetition Frequency versus Values of Capacitor C

Typical waveforms associated with this circuit are shown in Figure 17.

The duty cycle is less than 50 percent due to the internal $4\text{-k}\Omega$ resistor on the base of the input multi-emitter transistor, acting as a current source. If a 50 percent duty cycle is required the circuit may be modified as shown in Figure 18. Here the ratio of the discharge time-constant to charging time-constant is reduced by approximately $(1 + R_1/R_2)$, by including the additional feedback path formed by resistor R_1 and diode D_1 in parallel with resistor R_2 . For 50 percent duty cycle with

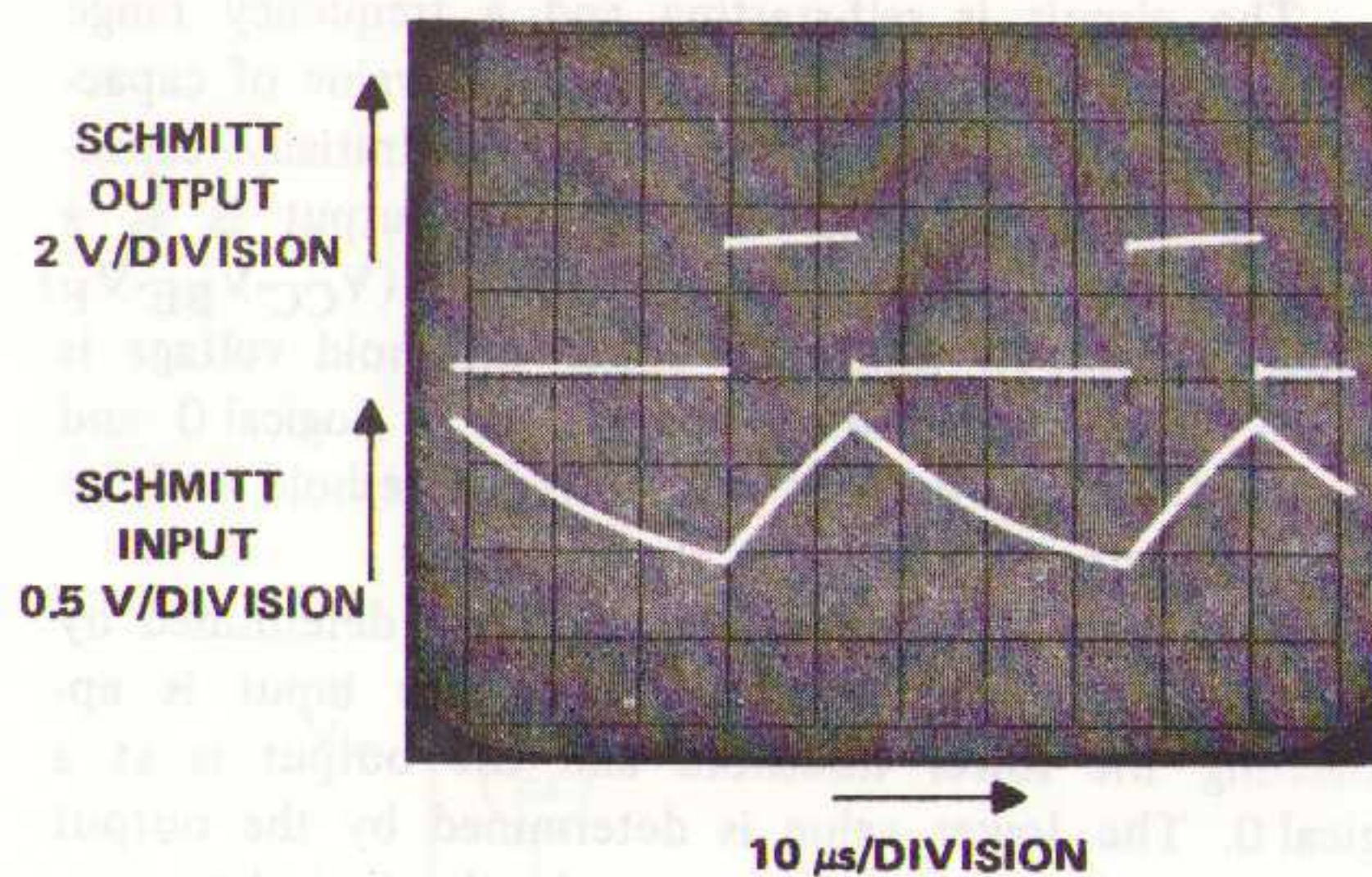


FIGURE 17. Typical Operating Waveforms for the Circuits in Figure 15

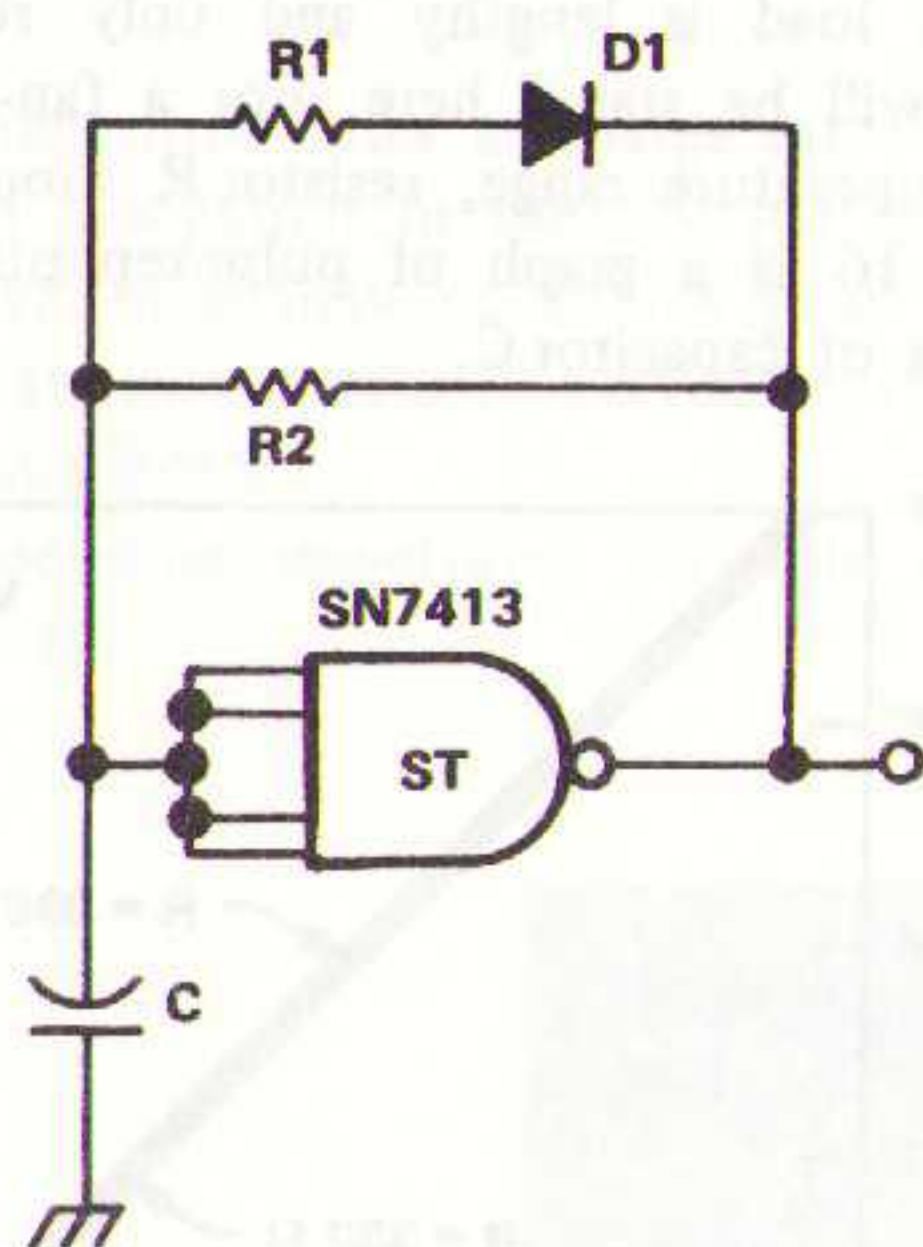


FIGURE 18. Circuit in Figure 15 Modified for 50 Percent Duty Cycle

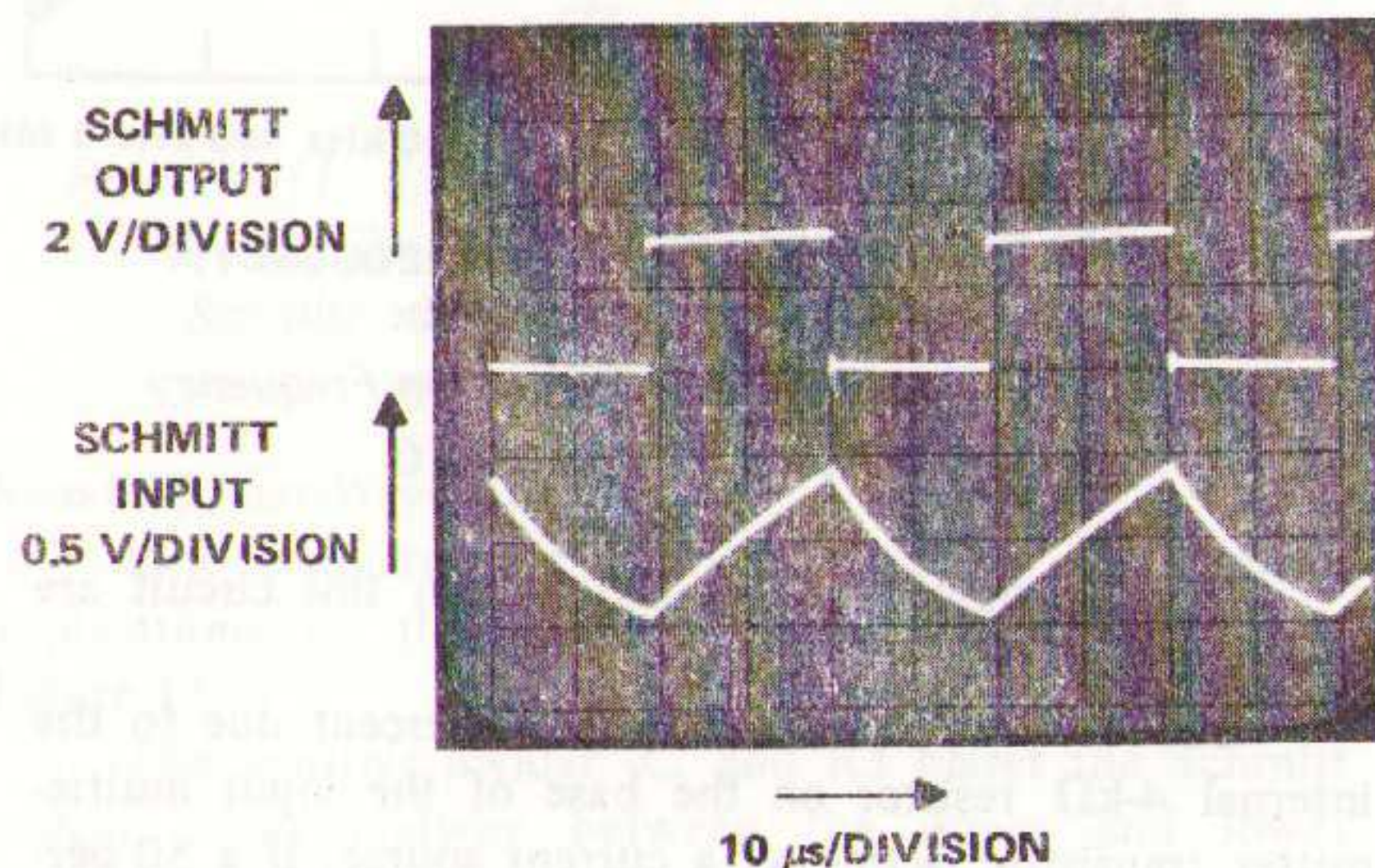


FIGURE 19. Typical Operating Waveforms for the Circuit in Figure 18.

$R_2 = 390\Omega$, R_1 should be 120Ω . The waveforms associated with this circuit are shown in Figure 19.

Gated Oscillator

The circuits of Figures 15 and 18 may be modified to function as gated multivibrators by the addition of an SN7401 open-collector NAND gate as shown in Figure 20.

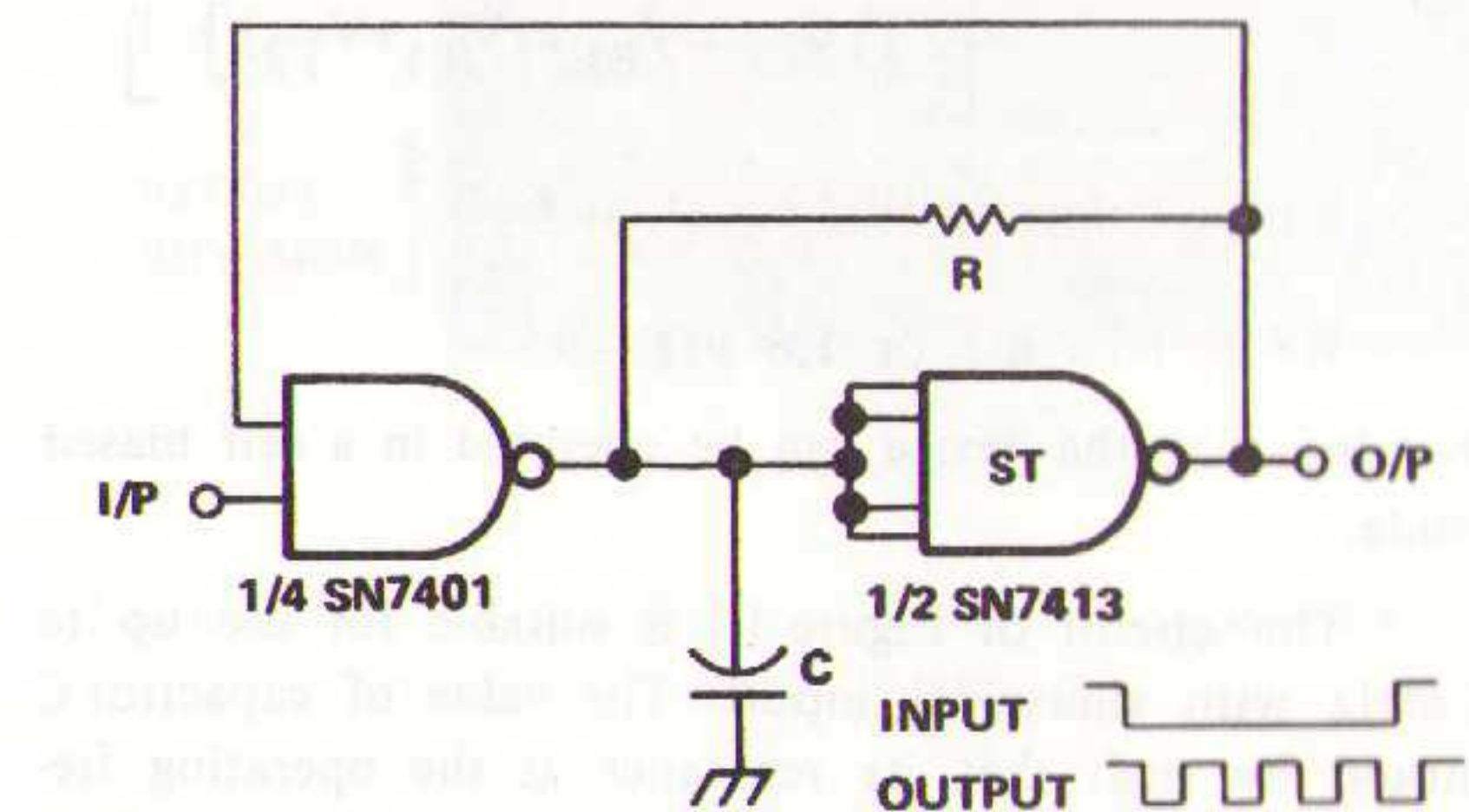


FIGURE 20. Circuits in Figure 15 and 18 Modified as Gated Oscillator

An additional feedback path from the output of the Schmitt to the input of the SN7401 prevents the gate signal from acting until the output of the SN7413 is at a logical 1. This ensures that the oscillator always produces an integral number of cycles.

Since the capacitor C has to charge from ground potential to the upper Schmitt trigger threshold before an output is produced, there is a delay between the positive-going edge of the start pulse and the beginning of the output-pulse train. In Figure 21 this time delay is plotted against value of capacitor C for R equal to 390Ω .

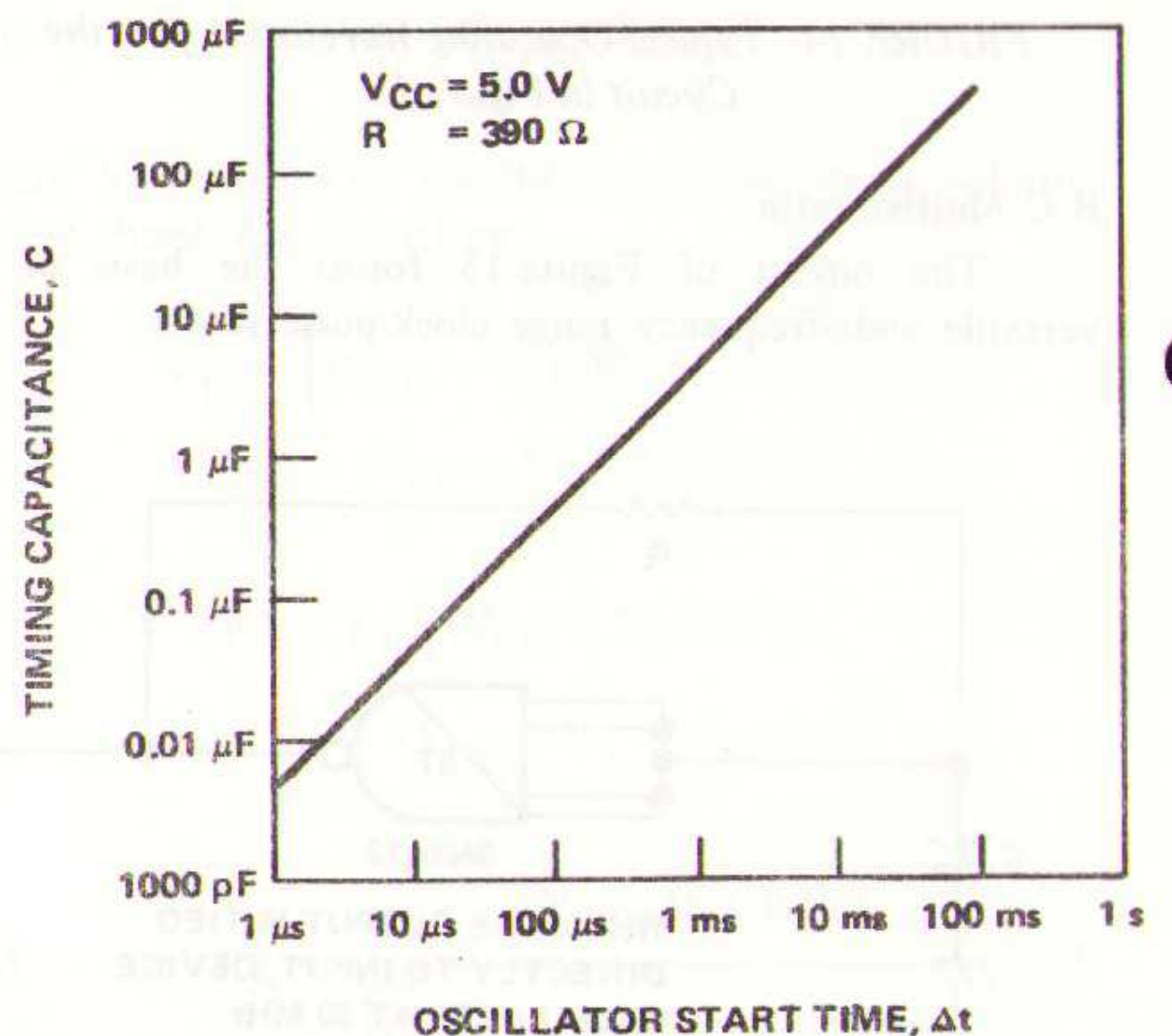


FIGURE 21. Graph of Oscillator Start Time versus Timing Capacitance

Typical operating waveforms associated with this circuit are shown in Figure 22.

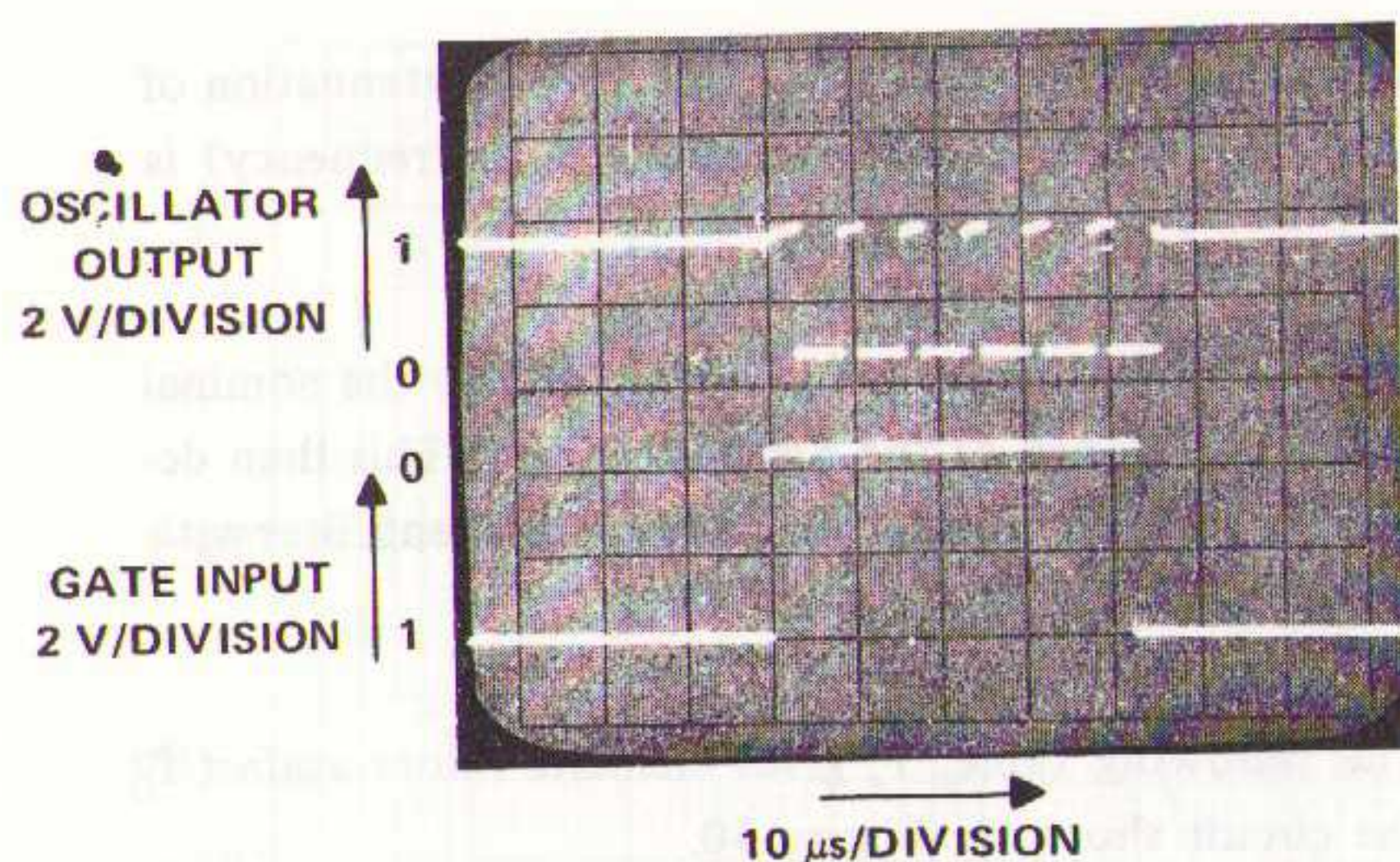


FIGURE 22. Typical Operating Waveform for Gated Oscillator in Figure 20

Edge Detector

A useful digital circuit is the edge detector or pulse differentiator. The SN7413 can perform this function with a minimum of external components. The circuit shown in Figure 23 has been, in the past, implemented with standard TTL but suffered from poor noise immunity and high-frequency instability.

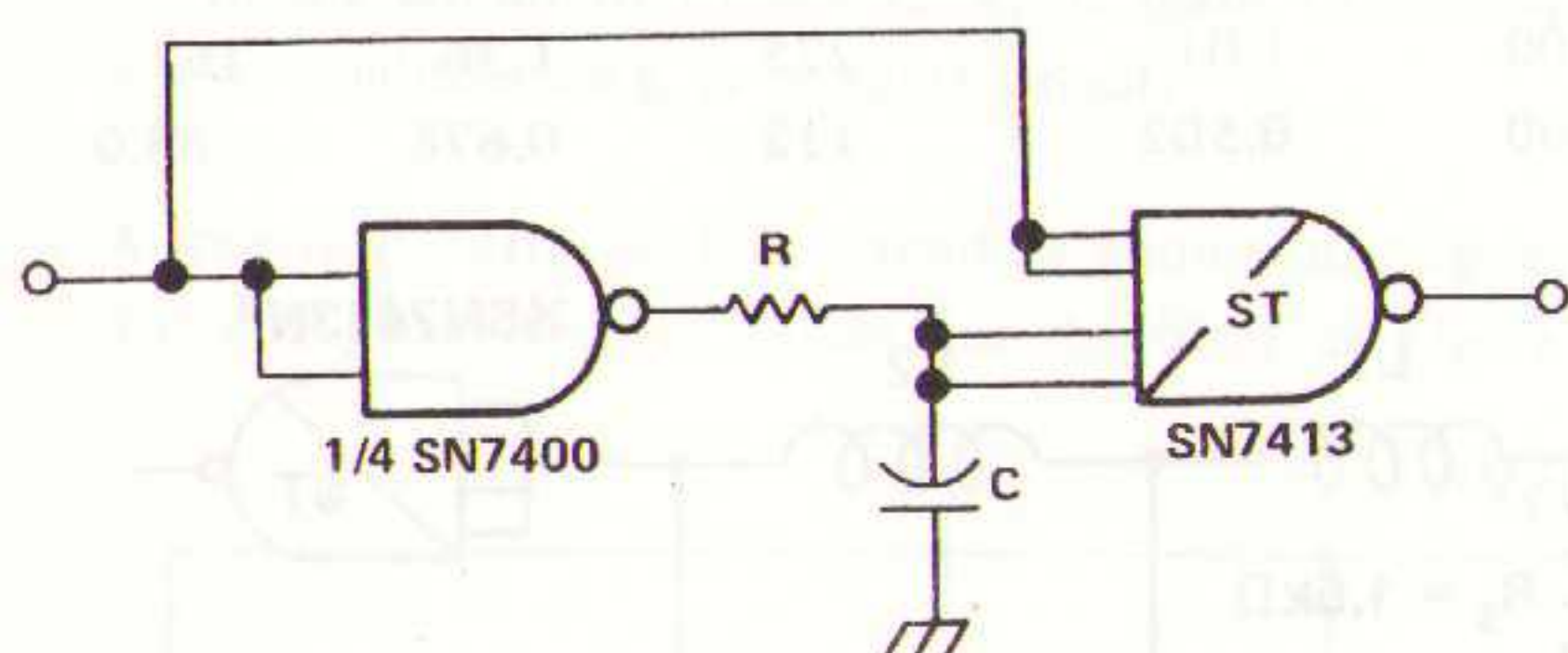


FIGURE 23. SN7413 Used in an Edge Detector Circuit or Pulse Differentiator

Figure 24 shows the operating waveforms associated with the circuit of Figure 23.

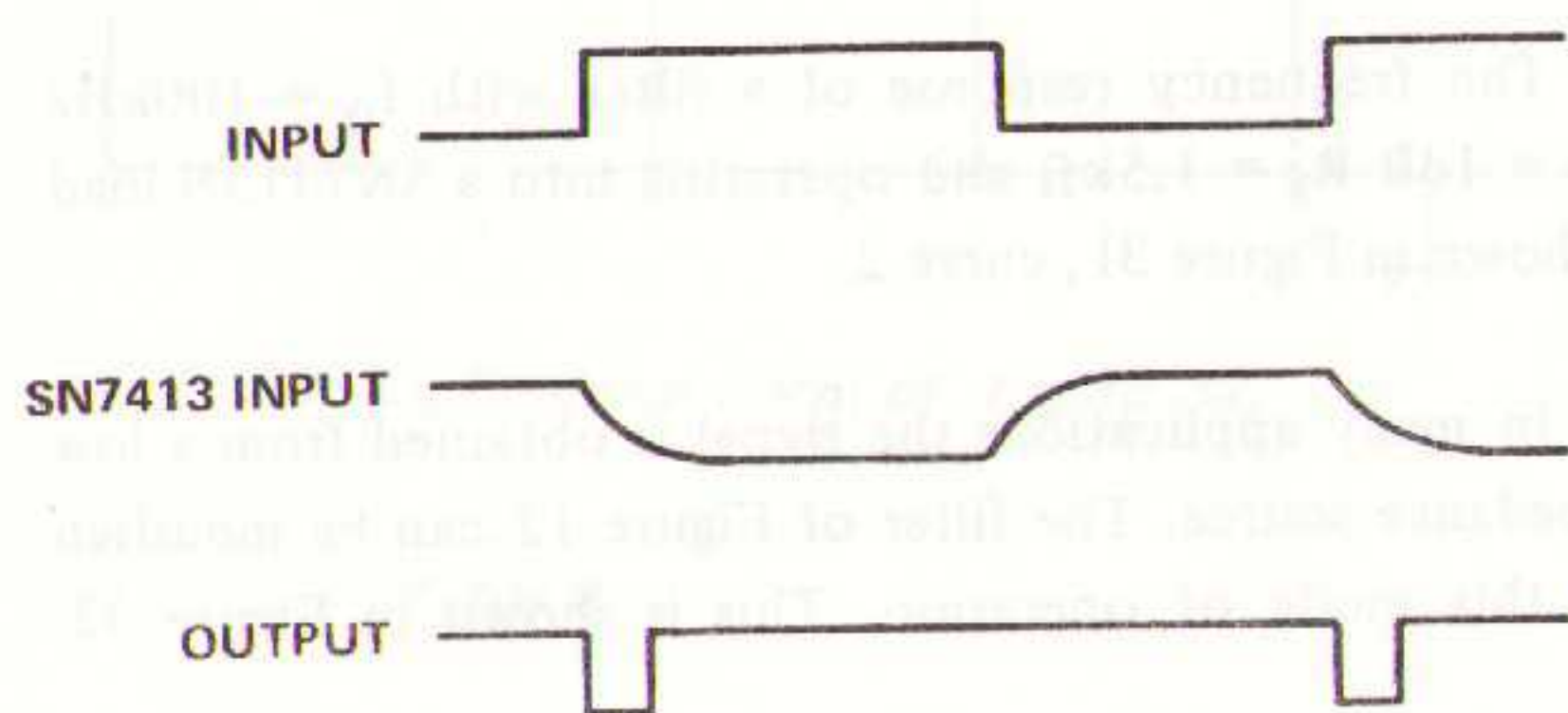


FIGURE 24. Operating Waveforms for the Circuit in Figure 23

Figure 25 indicates the range of pulse widths obtainable with this circuit.

A simple circuit, but of lower noise immunity is shown in Figure 26. This circuit operates on a logical 1 to logical 0 transition.

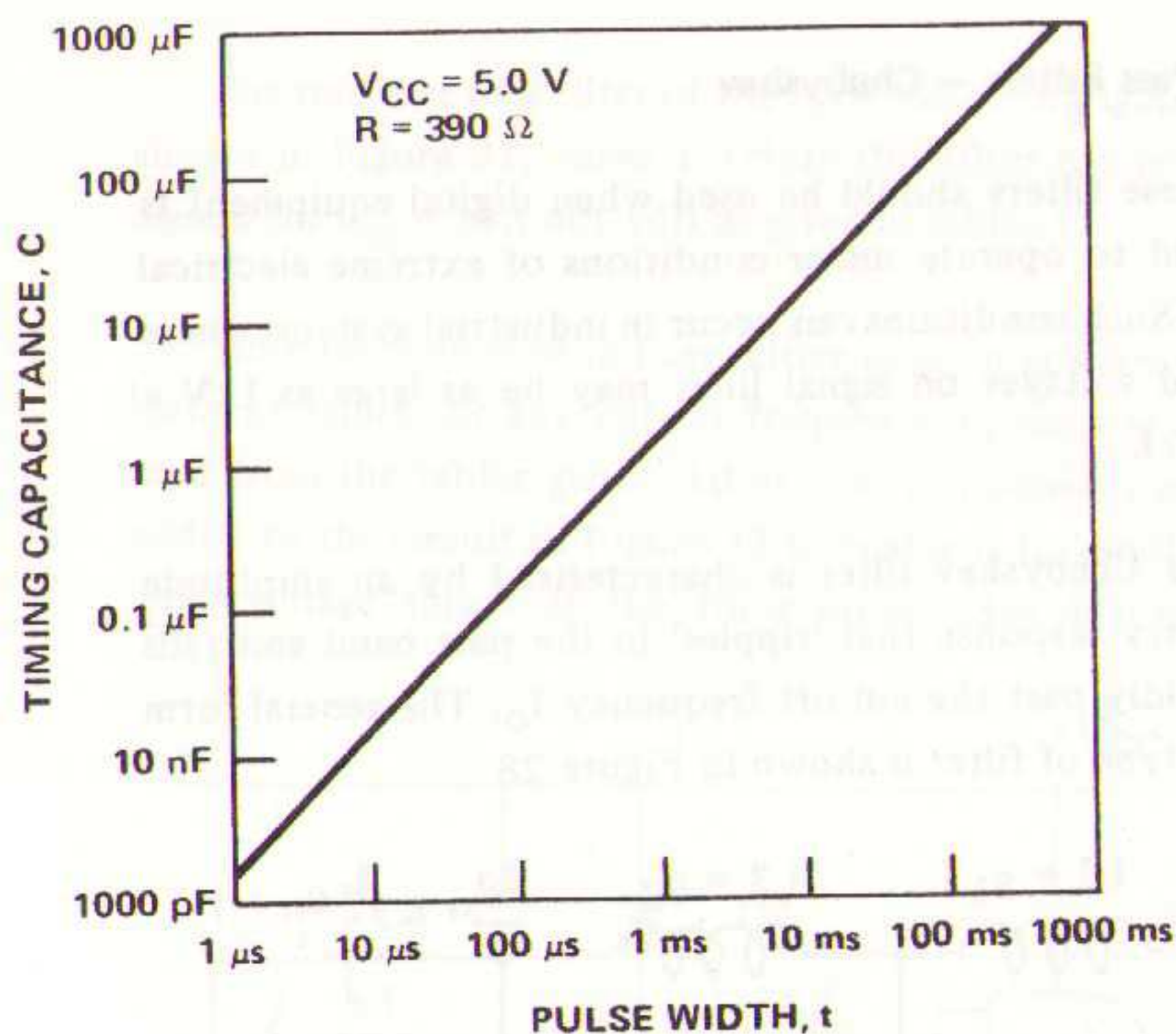


FIGURE 25. Graph of Timing Capacitance versus Pulse-Width for the Circuit in Figure 23

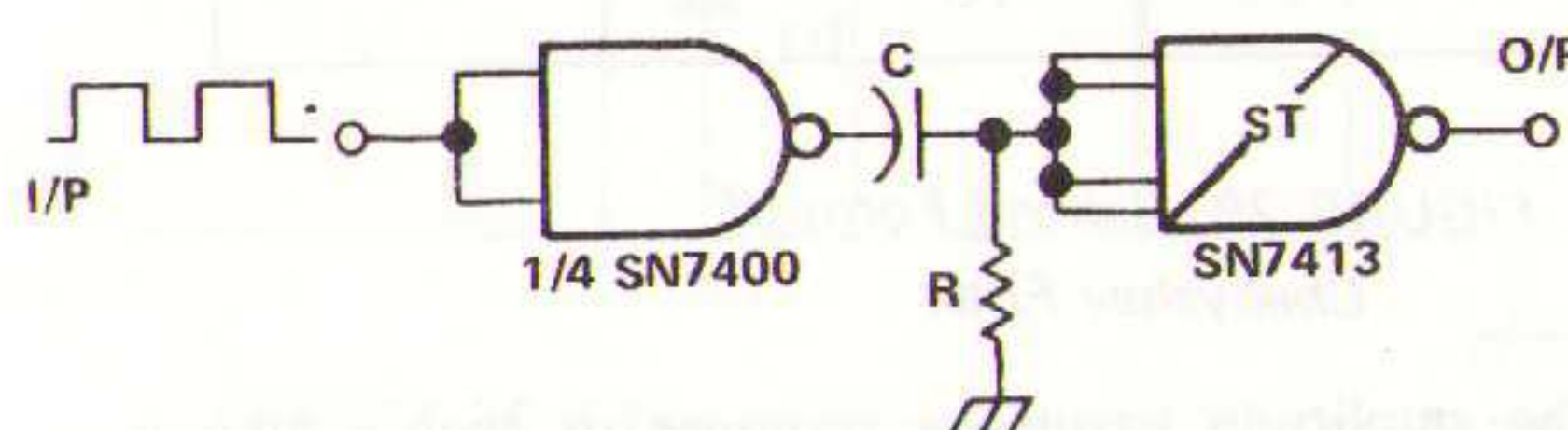


FIGURE 26. A Simple Edge Detector

The input Schmitt trigger is biased at the upper threshold voltage by resistor R. The input current at the upper threshold is $\approx -0.65\text{mA}$ giving a minimum value of resistor $R = 2.6\text{ k}\Omega$ for an upper threshold voltage of 1.7 V.

Low Pass Filters — Simple CR

The filter shown in Figure 27 is all that is needed, in the majority of cases, to eliminate noise associated with input signals. To maintain noise immunity at the Schmitt input the maximum value of resistor R should be limited as outlined in the section on pulse shaping. This, therefore, determines the value of capacitor C for a given 3dB cut-off frequency, f_o , of the filter, i.e. $C = 1/2\pi Rf_o$. The rate of attenuation past the cut-off frequency is 6dB/octave. For larger rates of attenuation and faster response times multipole Chebyshev filters should be used as described in the next section. Since the input to the Schmitt is always positive with respect to ground capacitor C may be a large value electrolytic.

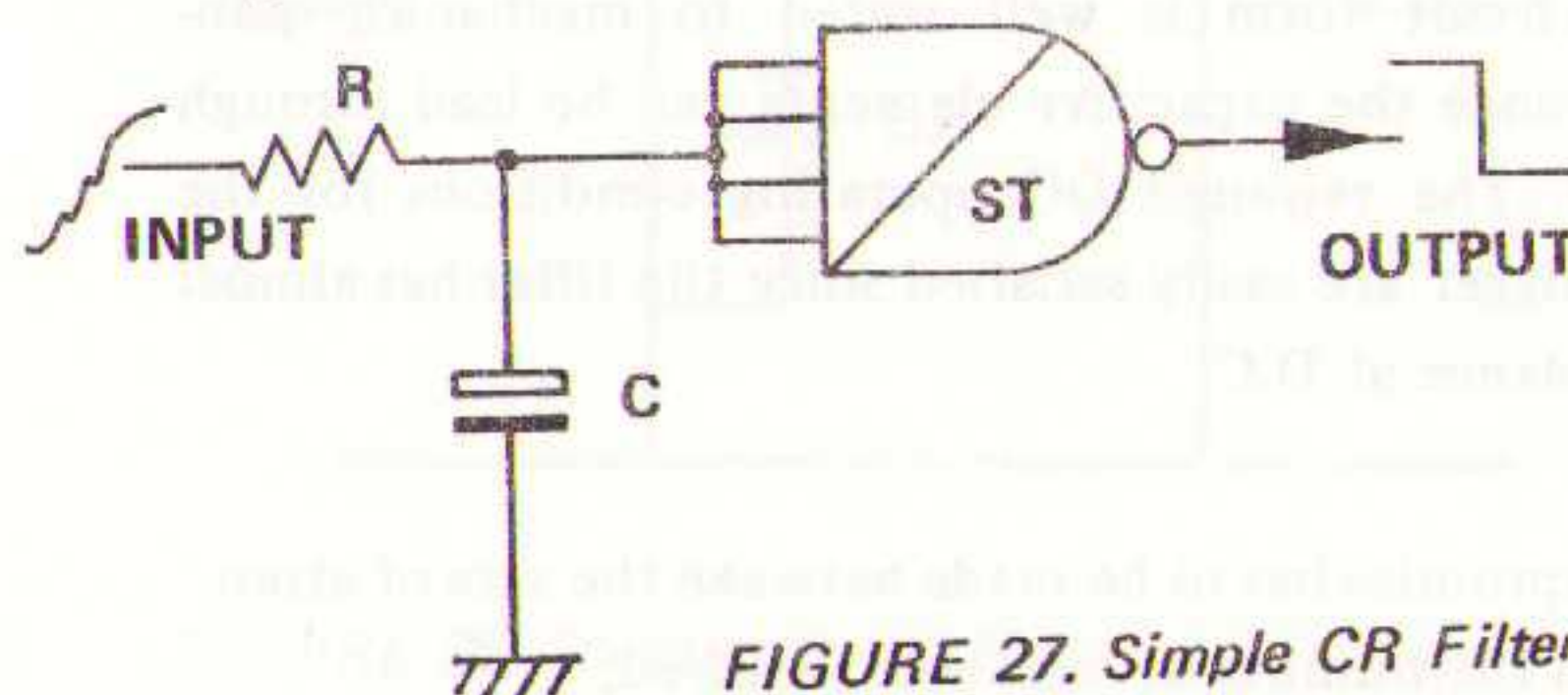


FIGURE 27. Simple CR Filter

Low Pass Filters — Chebyshev

These filters should be used when digital equipment is required to operate under conditions of extreme electrical noise. (Such conditions can occur in industrial systems where induced voltages on signal lines may be as large as 1kV at 500kHz).

The Chebyshev filter is characterised by an amplitude frequency response that 'ripples' in the pass band and falls off rapidly past the cut-off frequency f_o . The general form of this type of filter is shown in Figure 28

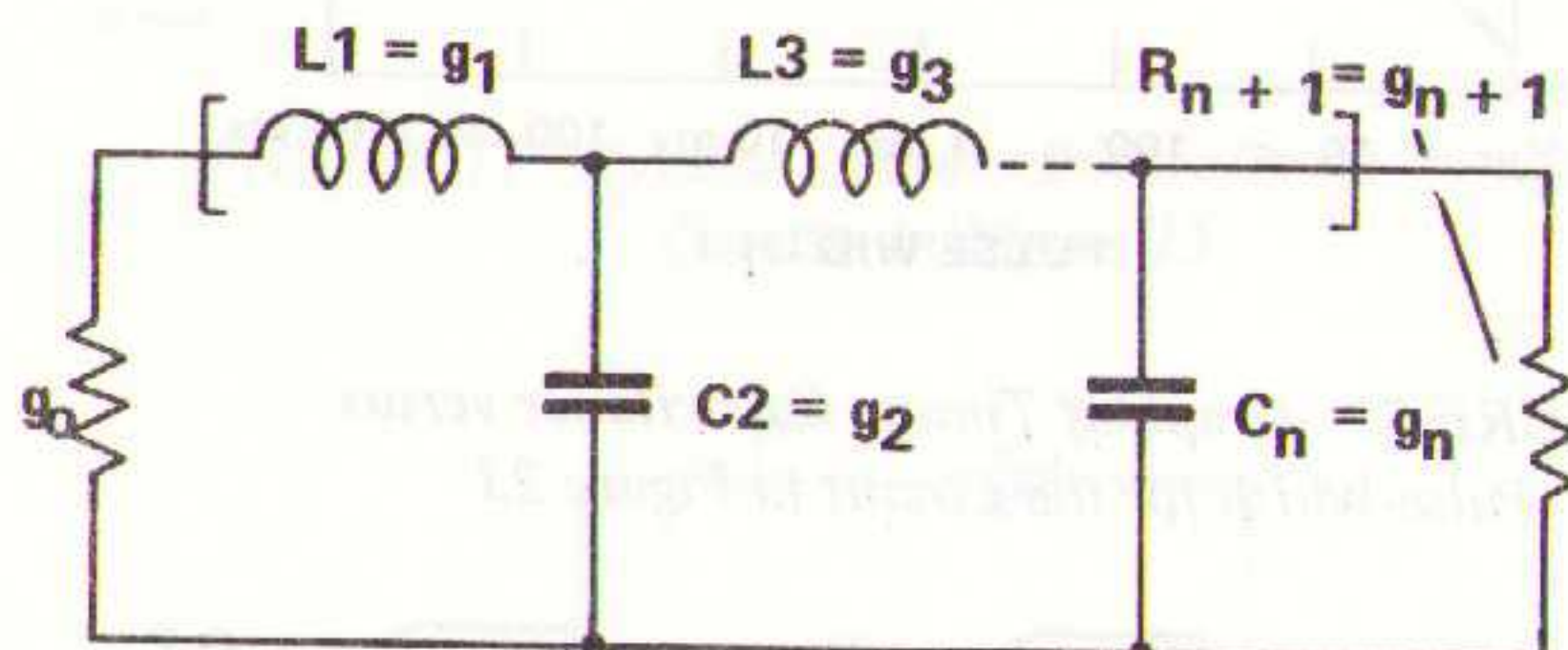


FIGURE 28. General Form of Chebyshev Filter

The amplitude frequency response of such a filter is shown in Figure 29

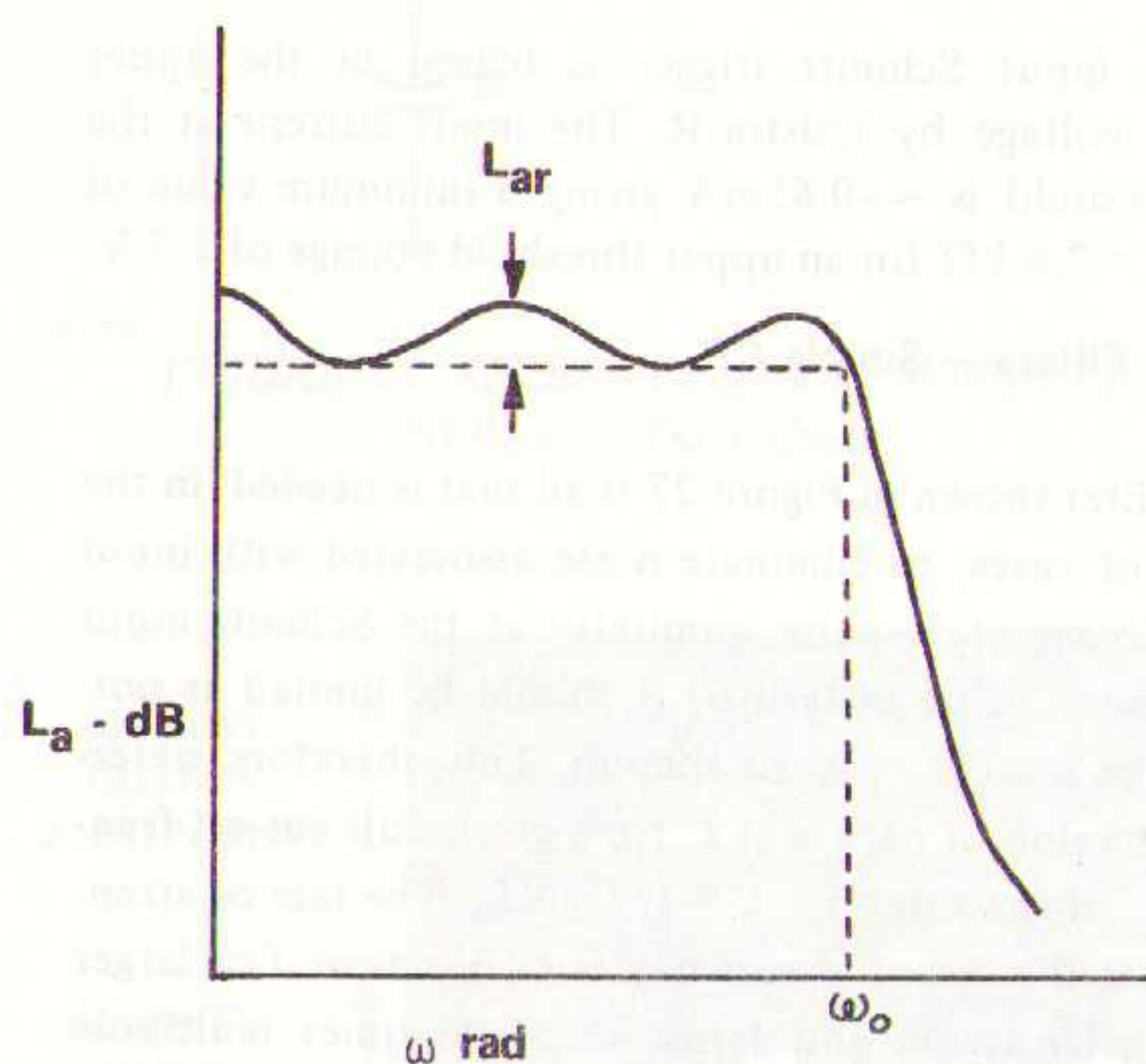


FIGURE 29. Amplitude Frequency Response

This circuit form is well suited to mechanical construction since the capacitive elements can be lead through capacitors. The required DC operating conditions for the Schmitt trigger are easily satisfied since the filter has almost zero impedance at D.C.

A compromise has to be made between the rate of attenuation and the number of elements required.

In practice a 4 element filter that has an attenuation of 60dB at $4\omega_o$ (where ω_o is the angular cut-off frequency) is useful.

The load resistance $R_n + 1$ is determined by the nominal 4kΩ input impedance of the Schmitt trigger. This then determines the source impedance g_o . For a 4 element filter with 1dB ripple in the pass band $g_o = 1.5k\Omega$.

The following table, 1, gives element values against f_o for the circuit shown in Figure 30.

Table 1

Element values for 4 element filter with $L_{ar} = 1\text{dB}$ and $L_a = -60\text{dB}$ at $4\omega_o$.

f_o (kHz)	L1(mH)	C1(pF)	L2(mH)	C2(pF)
100	5.02	1126	6.78	835
200	2.51	563	3.39	417
500	1.01	225	1.36	167
1000	0.502	112	0.678	83.0

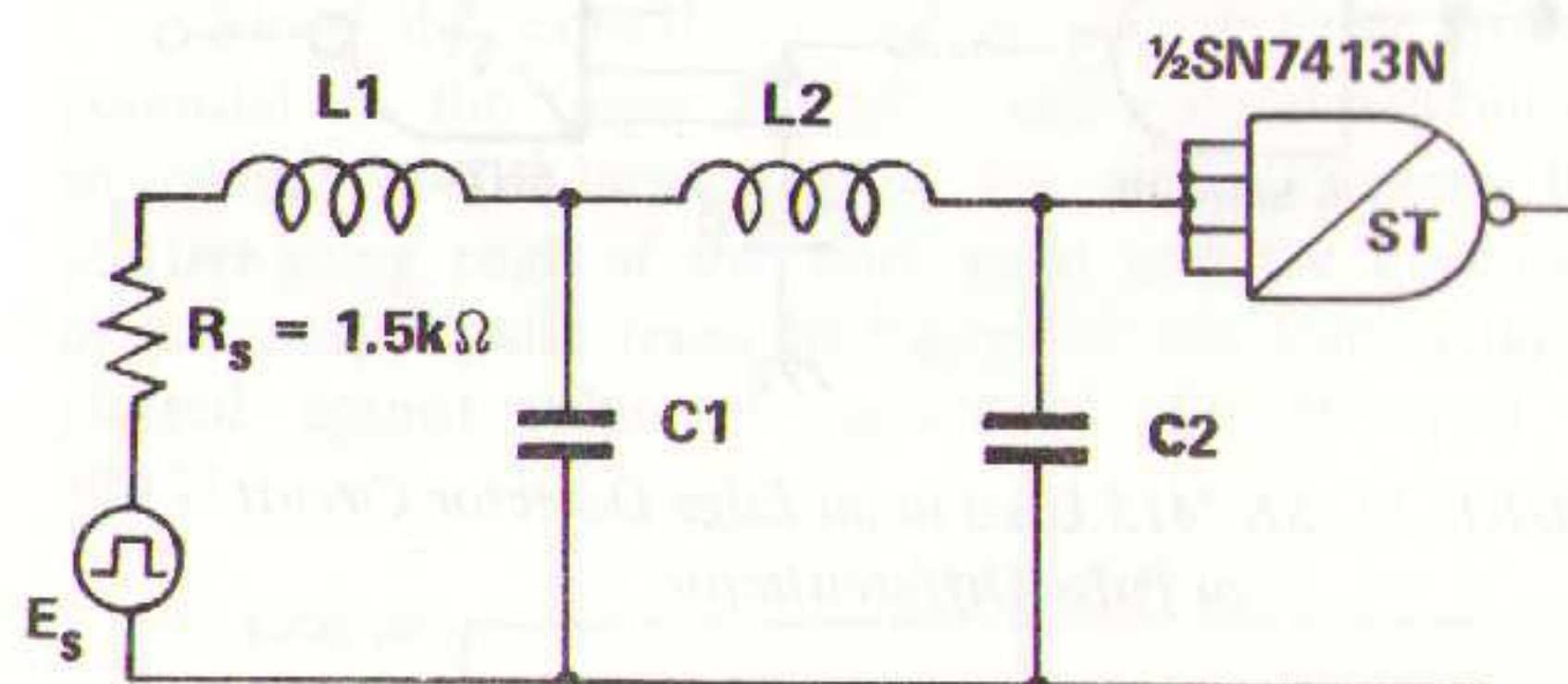


FIGURE 30. Four Element Filter

The frequency response of a filter with $f_o = 100\text{kHz}$, $L_{ar} = 1\text{dB}$, $R_s = 1.5k\Omega$ and operating into a SN7413N load is shown in Figure 31, curve 2.

In many applications the signal is obtained from a low impedance source. The filter of Figure 12 can be modified for this mode of operation. This is shown in Figure 32.

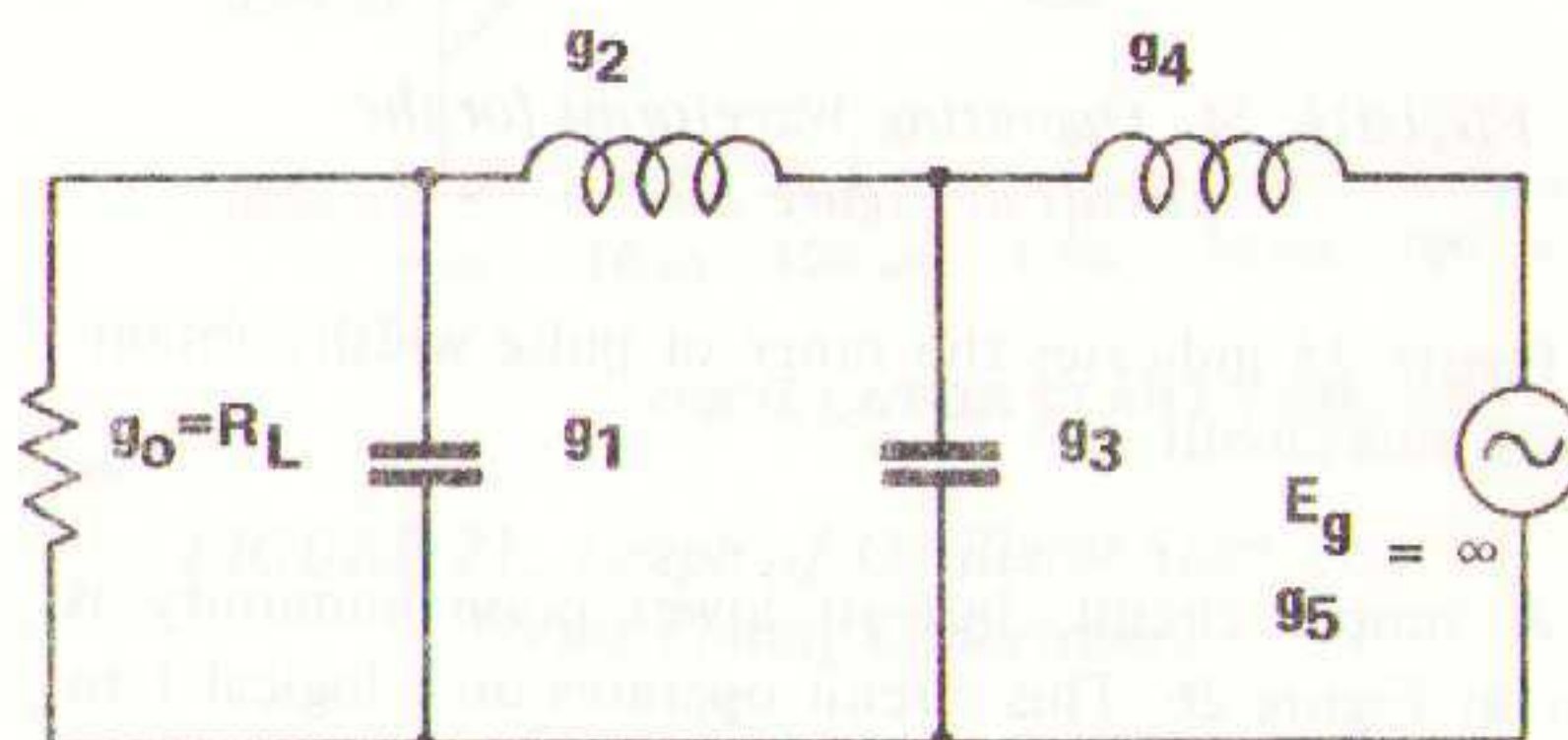


FIGURE 32. Filter Driven From Zero Source Impedance

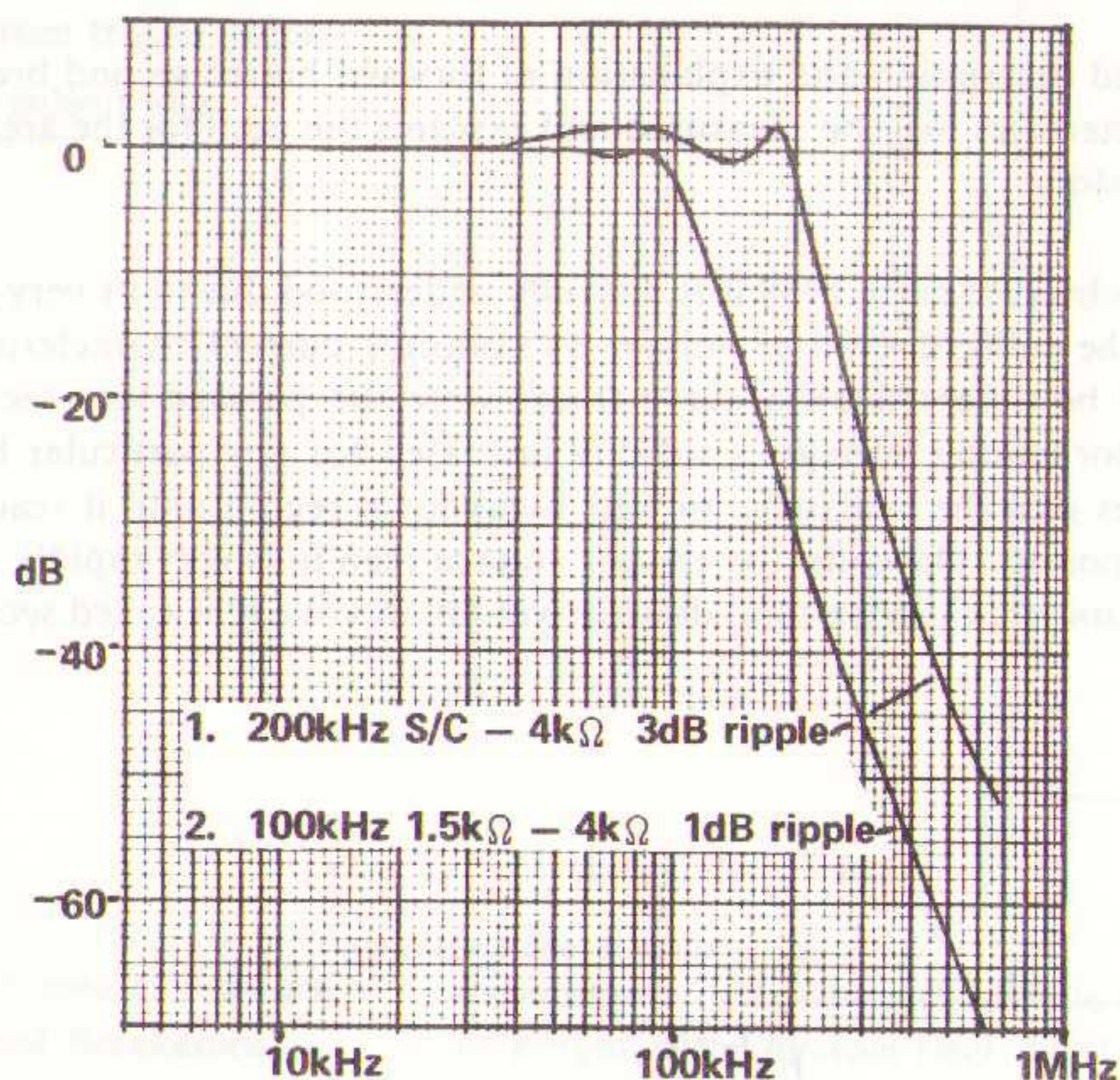


FIGURE 31. Low Pass Filter Characteristic

In the circuit of Figure 32 R_L is again 4.0kΩ and the source conductance g_s is ∞ (short circuit)

A practical form of this circuit is shown in Figure 33. Table 2 gives element values for the filter of Figure 33.

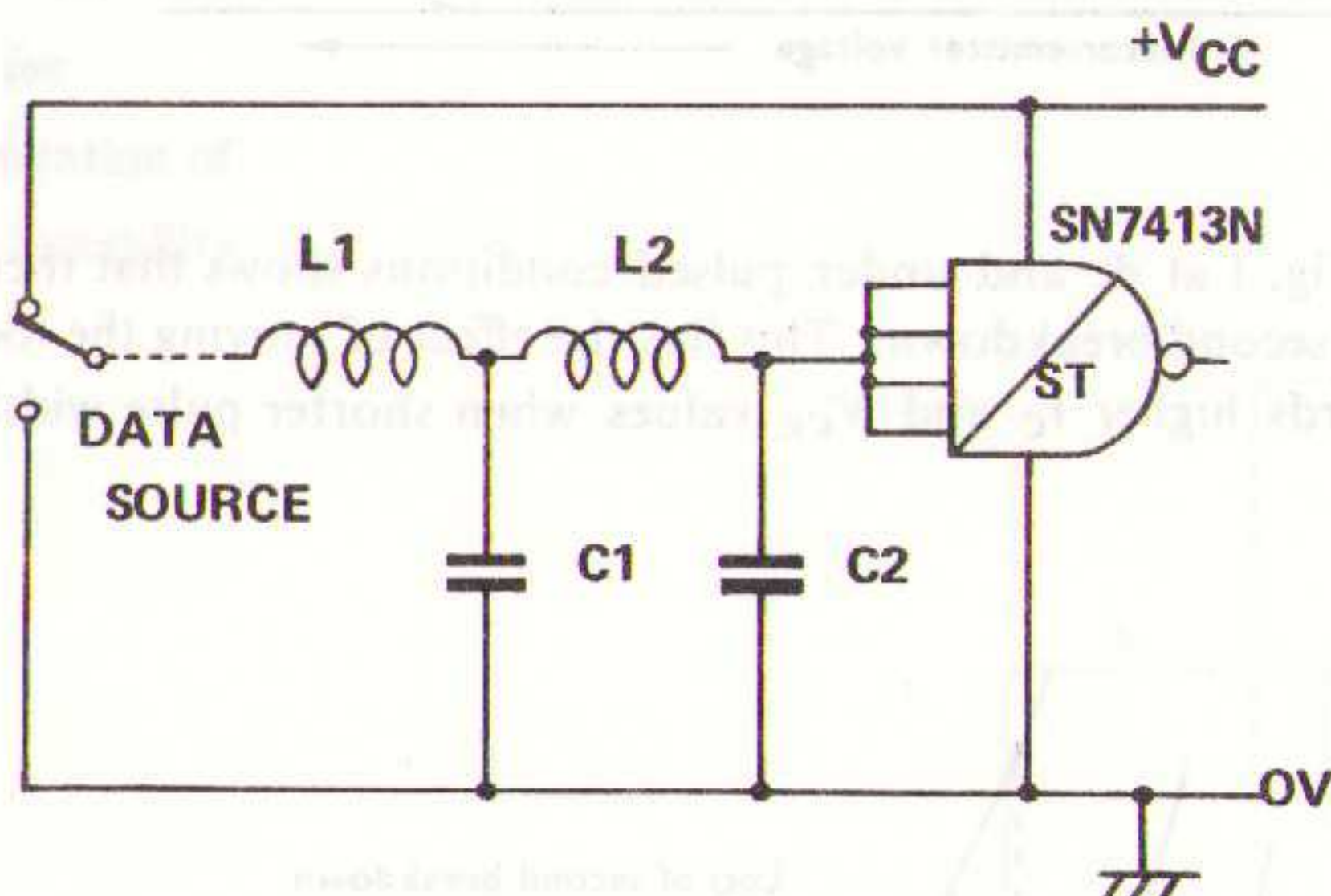


FIGURE 33. Practical Form of Figure 32.

Table 2

Element values for 4 element filter with $L_{ar} = 1\text{dB}$ and $L_a = -60\text{dB}$ at $4 \omega_0$.

f_0 (kHz)	L1(mH)	C1(pF)	L2(mH)	C2(pF)
100	8.99	417	8.16	760
200	4.50	2209	4.08	379
500	1.80	83.5	1.63	152
1000	0.90	41.8	0.816	76.0

The response of a filter of the type shown in Figure 33 is shown in Figure 31, curve 1. (Note this filter has been designed for $L_{ar} = 3\text{dB}$ not 1dB as given in tables.)

Since the inductive and capacitive components are $\propto 1/f$ element values for any cut-off frequency f_0 may be calculated from the tables given. Additional components may be added to the circuit of Figure 33 to enable it to handle very large voltage surges at the filter input. (See Figure 34).

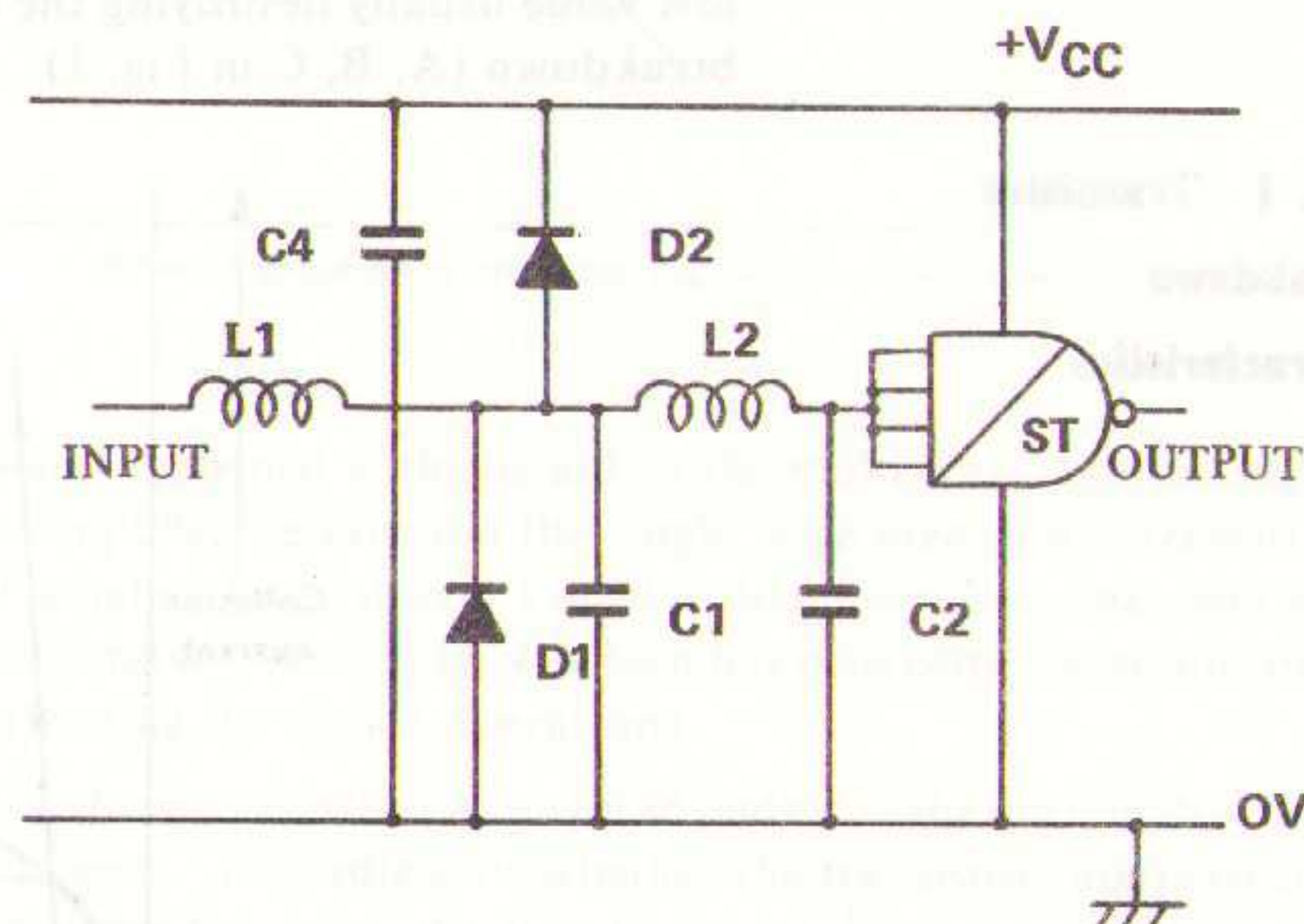


FIGURE 34. Filter to Handle Large Voltage Surges

Diodes D1 and D2 clamp the input to the Schmitt trigger to within $(V_{CC} - V_F)$ and $-V_F$. They should be situated after inductor L1 so that the rate of rise of voltage across diodes D1 and D2 is limited.

The filters described in the previous sections can be constructed as shown in Figure 35; this gives a large degree of isolation between various elements.

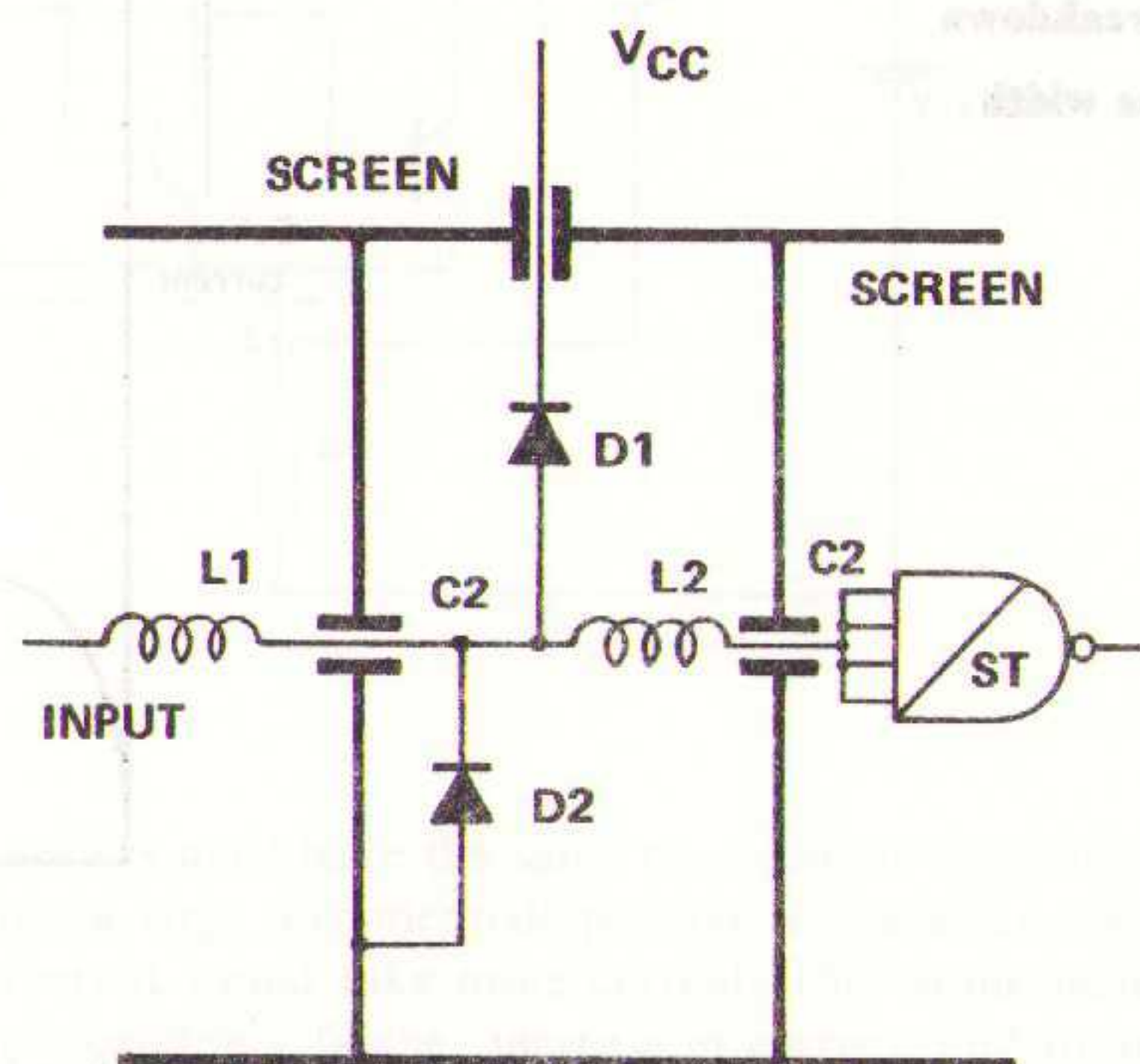


FIGURE 35. Constructional Form

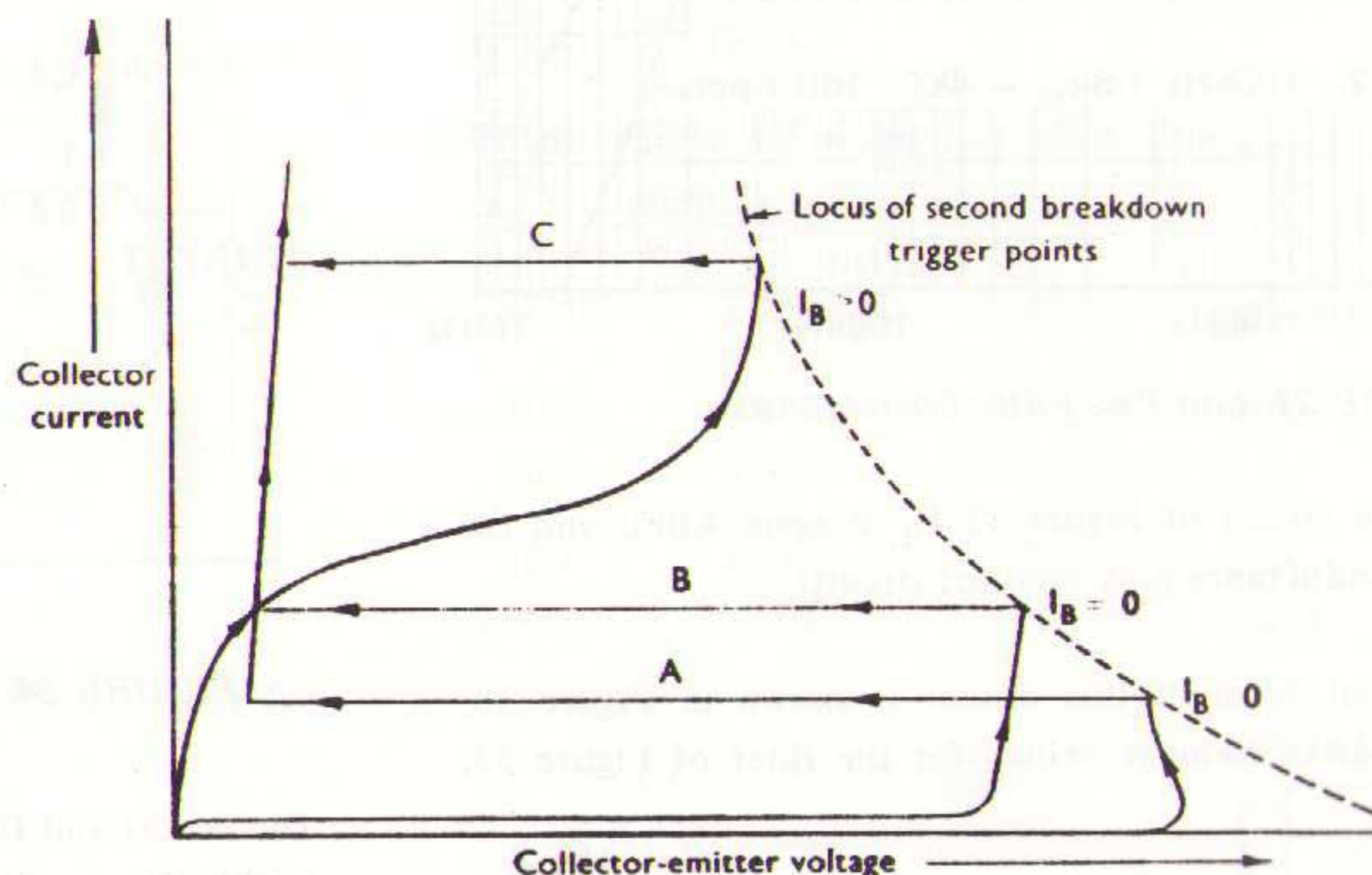
Introduction

This note is intended to give a simplified description and explanation of forward biased second breakdown. It then shows how these characteristics may be measured and explains the need for the area of operation specification of power transistors.

Description of Second Breakdown

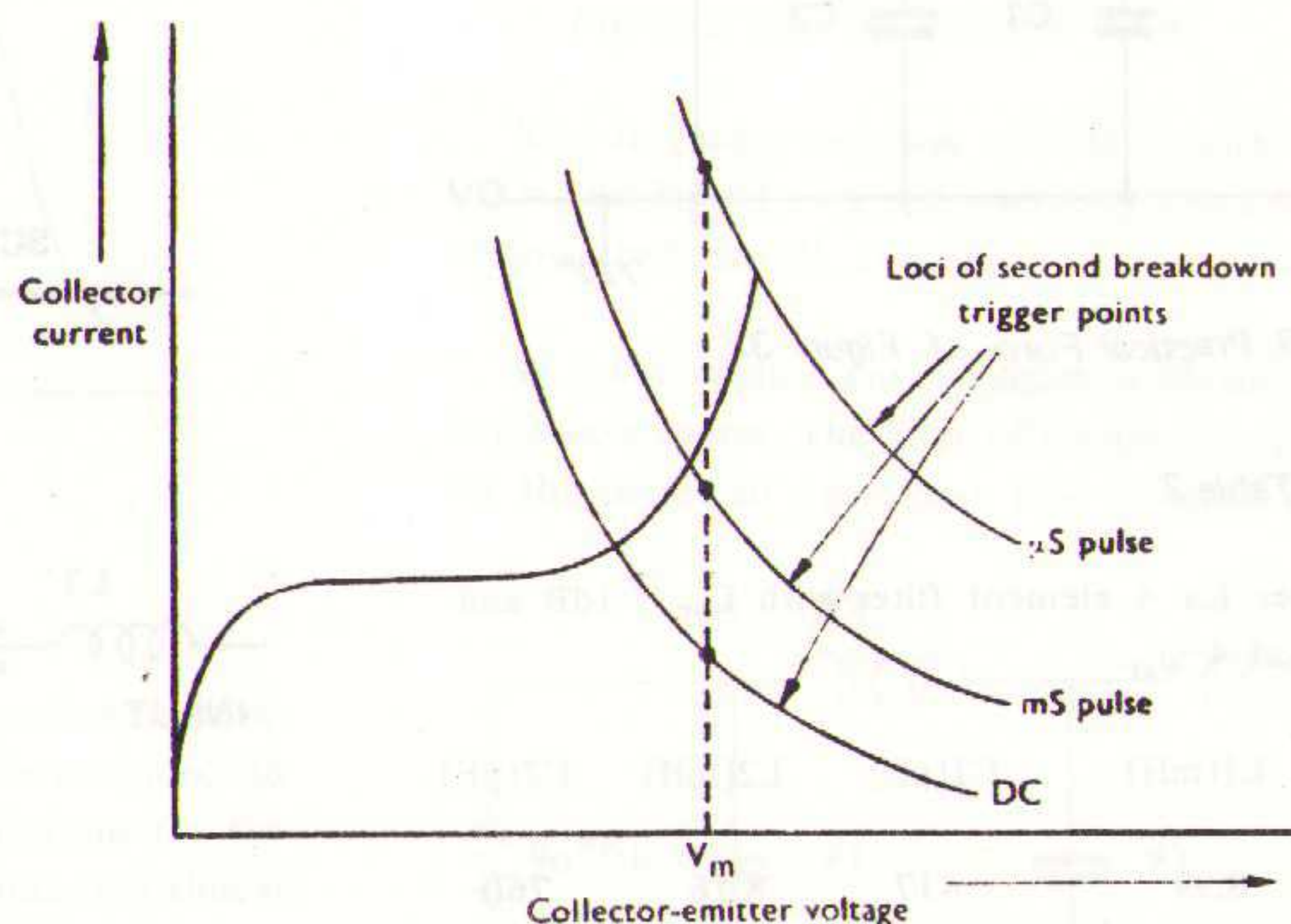
Although second breakdown has been observed since 1958 it is not fully understood due to its very fast and destructive nature. Fig. 1 shows the collector-emitter voltage vs collector current characteristics of a typical transistor—such as could be observed on a curve tracer were the passage into second breakdown not destructive. As collector-emitter voltage is steadily increased for any particular base drive condition the characteristic passes into the avalanche or first breakdown region until it reaches the locus of second breakdown trigger points. The collector-emitter voltage then falls very rapidly to a low value usually destroying the transistor, this sudden (and destructive) fall in voltage is called second breakdown (A, B, C in Fig. 1).

Fig. 1 Transistor breakdown characteristics



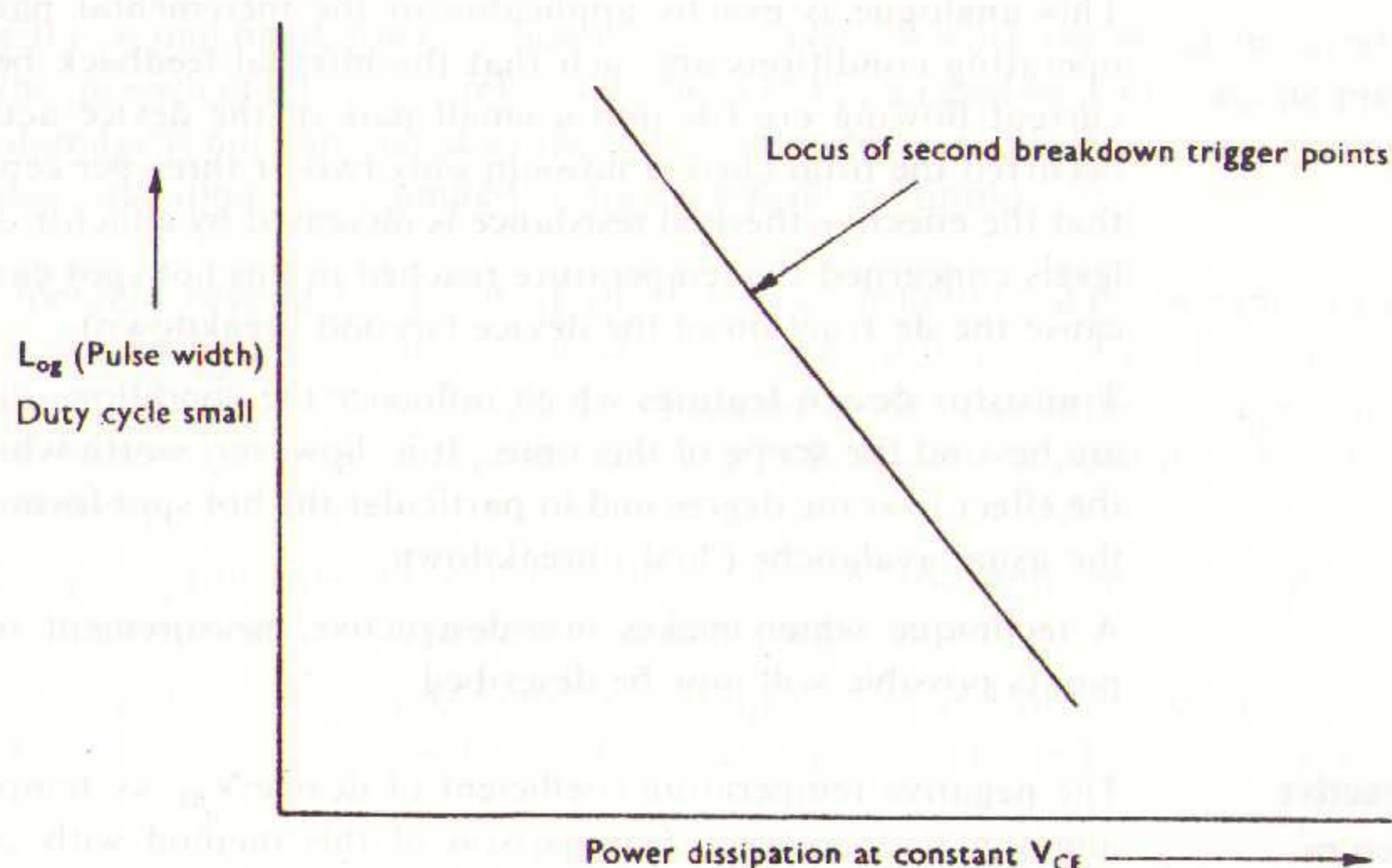
Investigation of characteristics such as Fig. 1 at dc and under pulsed conditions shows that there is a finite time delay before the device enters second breakdown. This has the effect of moving the locus of second breakdown trigger points towards higher I_C and V_{CE} values when shorter pulse widths are used—See Fig. 2.

Fig. 2 Variation of second breakdown with pulse width



There is a simple relationship between the power levels (currents) at which second breakdown occurs with forward bias at constant voltage and varying time—shown by V_m in Fig. 2. The relationship between trigger power and pulse width is further plotted in Fig. 3.

Fig. 3 The relation between trigger point and pulse width

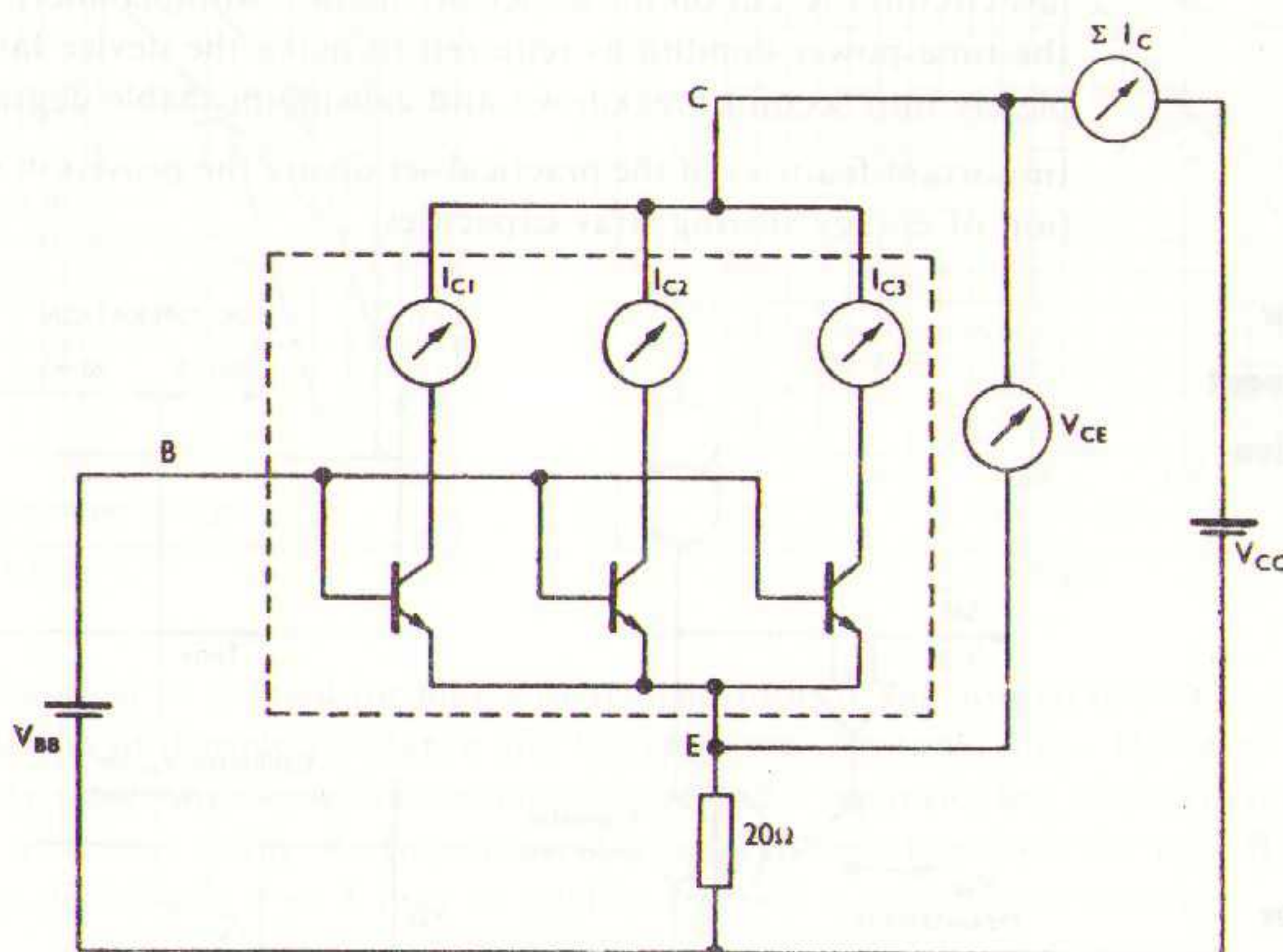


The Cause of Forward Second Breakdown

The cause of second breakdown is most easily explained with the aid of the multi transistor analogue of Bergman & Gerstner (Ref. 1). For this simplified description the single large area power transistor is represented by three separate paralld smaller transistors. For the demonstration the paralld devices have common base drive in a current limited circuit (Fig. 4) which has provision for monitoring the individual collector currents (without affecting the device operation)

If one now applies current and voltage to the three transistor circuits one finds that the current distribution varies with time as described in the reference. Regardless of whether the transistors are perfectly matched or not, once the total dissipation exceeds a critical value the (lateral) current distribution between the devices becomes unstable and one device hogs most of the current.

Fig. 4 Transistor model for demonstration of lateral instability



This is explained by the fact that all three devices must have the same base emitter bias (in parallel) but the collector current for a given V_{BE} has a large (exponential) positive temperature coefficient. Thus if any device were hotter than the others it would take more current. This would increase its dissipation and hence its junction temperature, causing a further increase in current, and so on. The result of this positive feedback is that one device will take nearly all the current.

It is significant that once the feedback is overcritical the current distribution will be unstable regardless of matching defects.

This analogue is exactly applicable to the incremental parts of a single large transistor. Once the operating conditions are such that the internal feedback becomes overcritical the greater part of the current flowing crowds into a small part of the device active area. Once this lateral instability has occurred the total current flows in only two or three per cent (or less) of the active area with the result that the effective thermal resistance is increased by a factor of 50 to 100 times. According to the power levels concerned the temperature reached in this hot spot can easily be sufficient to melt the silicon and cause the destruction of the device (second breakdown).

Transistor design features which influence the conditions under which this hot spot formation occurs are beyond the scope of this note. It is, however, worth while observing that all transistors suffer from the effect to some degree and in particular the hot spot formation can occur at voltage levels well below the usual avalanche ('first') breakdown.

A technique which makes non-destructive measurement of the locus of second breakdown trigger points possible will now be described.

The Non-Destructive Characterisation of Second Breakdown and Thermal Resistance

The negative temperature coefficient of device V_{BE} vs temperature provides a convenient measure of junction temperature. Comparison of this method with an infra-red microradiometer shows that correct techniques produce negligible errors. For example, the dc thermal resistance may be measured by the application of dc power to the device on a suitable heat sink and interrupting this power for a few hundred micro seconds to measure V_{BE} under calibrated conditions. Provided measurement starts within a few microseconds of the power cut off it will be accurate.

If hot spot formation has started the V_{BE} measurement will monitor the thermal decay of the small hot region and time constants typically as short as 25 microseconds have been observed.

A further consequence of hot spot formation is that both junction temperature and current density (in the hot region) increase. The net effect is that V_{BE} falls by a few tens of millivolts but can no longer be used as an accurate measure of junction temperature.

According to device type and conditions, this V_{BE} change may occur in times of the order micro seconds to milli seconds. Of course, destruction will follow if the energy levels are sufficiently great.

The technique used for characterisation of second breakdown is to sense the V_{BE} drop and to provide fast circuitry to cut off the device dissipation within a microsecond or two of this. Thus we can measure the time-power conditions required to make the device laterally unstable without ever taking it completely into second breakdown and causing probable degradation.

Important features of the practical set up are the provision of current limited sources and the minimisation of energy storing stray capacities.

Fig. 5 Transistor thermal measurement circuit configuration

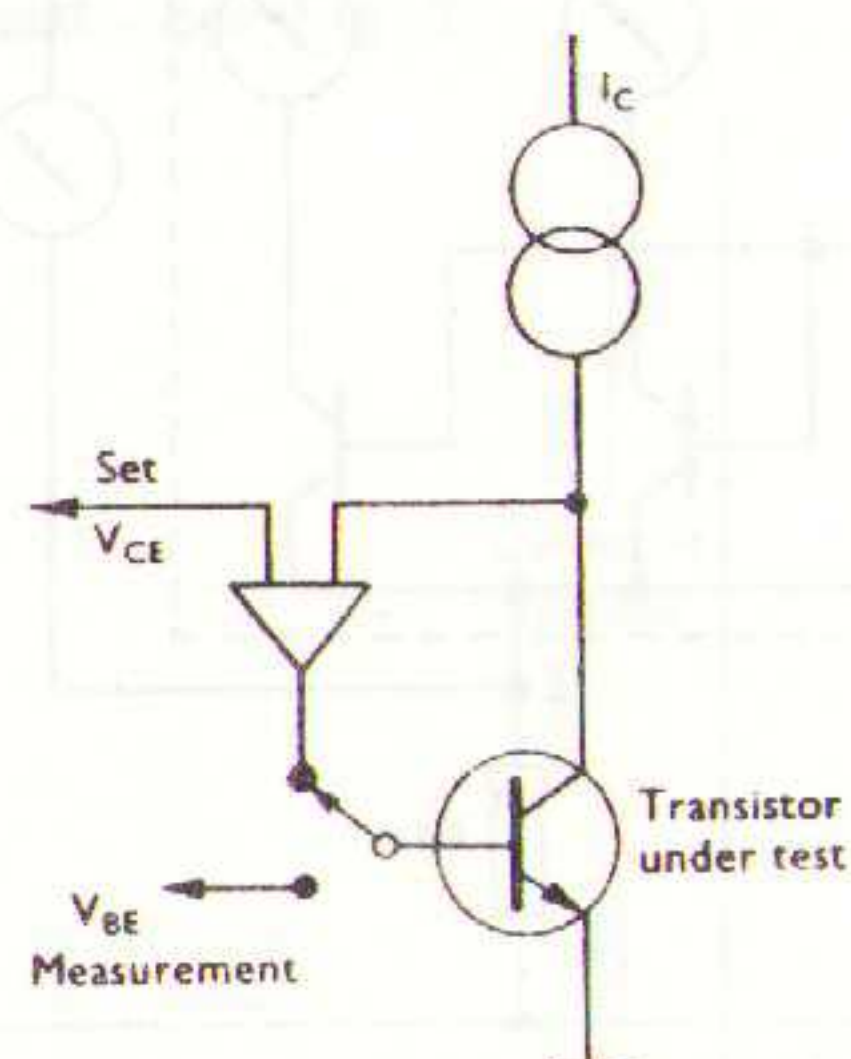


Fig. 6 Transistor thermal measurement waveforms

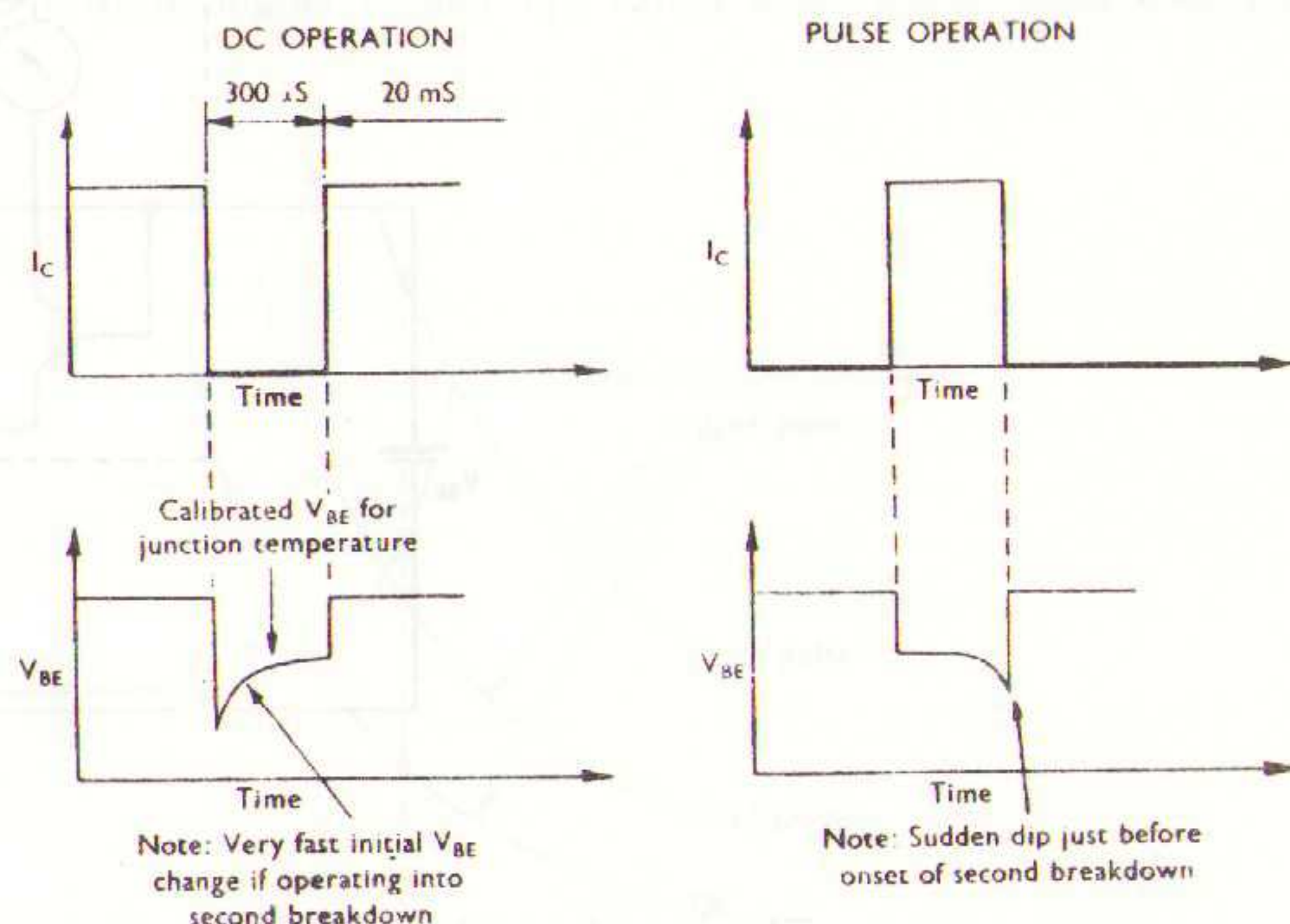


Fig. 5 shows the system arrangement used for thermal and second breakdown evaluation, especially for Texas Instruments VHF Power Devices. The waveforms obtained in practice are shown in Fig. 6. For dc operation the repetition rate becomes 50 c/s and duty cycle about 98.5%.

Summary—Maximum Area of Operation

A second technique for second breakdown evaluation is possible—to work the device in current limited circuitry and have the 'power cut off sensor' rely on the drop in V_{CE} caused by actual second breakdown. In this case device damage is not eliminated as the hot spot temperature must reach a very high value. One advantage is that operation is not limited to forward bias conditions.

A device may be operated beyond the point at which lateral instability starts without catastrophic failure. However, operation in this mode cannot be recommended in view of the fact that control of junction temperature is virtually lost. A few per cent increase in dissipation beyond the critical point can result in several hundred degrees centigrade increase in junction temperature—a feature hardly likely to result in longevity.

It is therefore most important that the transistor specification shall give sufficient information to enable the user to be certain that the device is operated in a stable region.

Ideally the specification will include a maximum 'area of operation' and thermal derating which must be used together. Figs 7 and 8 are examples of these characteristics for a hypothetical VHF power transistor.

Fig. 7 shows the maximum 'area of operation' which has two separate regions—A, in which operation is straightforward dissipation (or thermally) limited, and B, in which operation is limited by second breakdown.

Provided the device is operated within the specified limits there will be no significant hot spot formation and reliable service should be achieved.

Fig. 7, 8 Safe Area of Operation

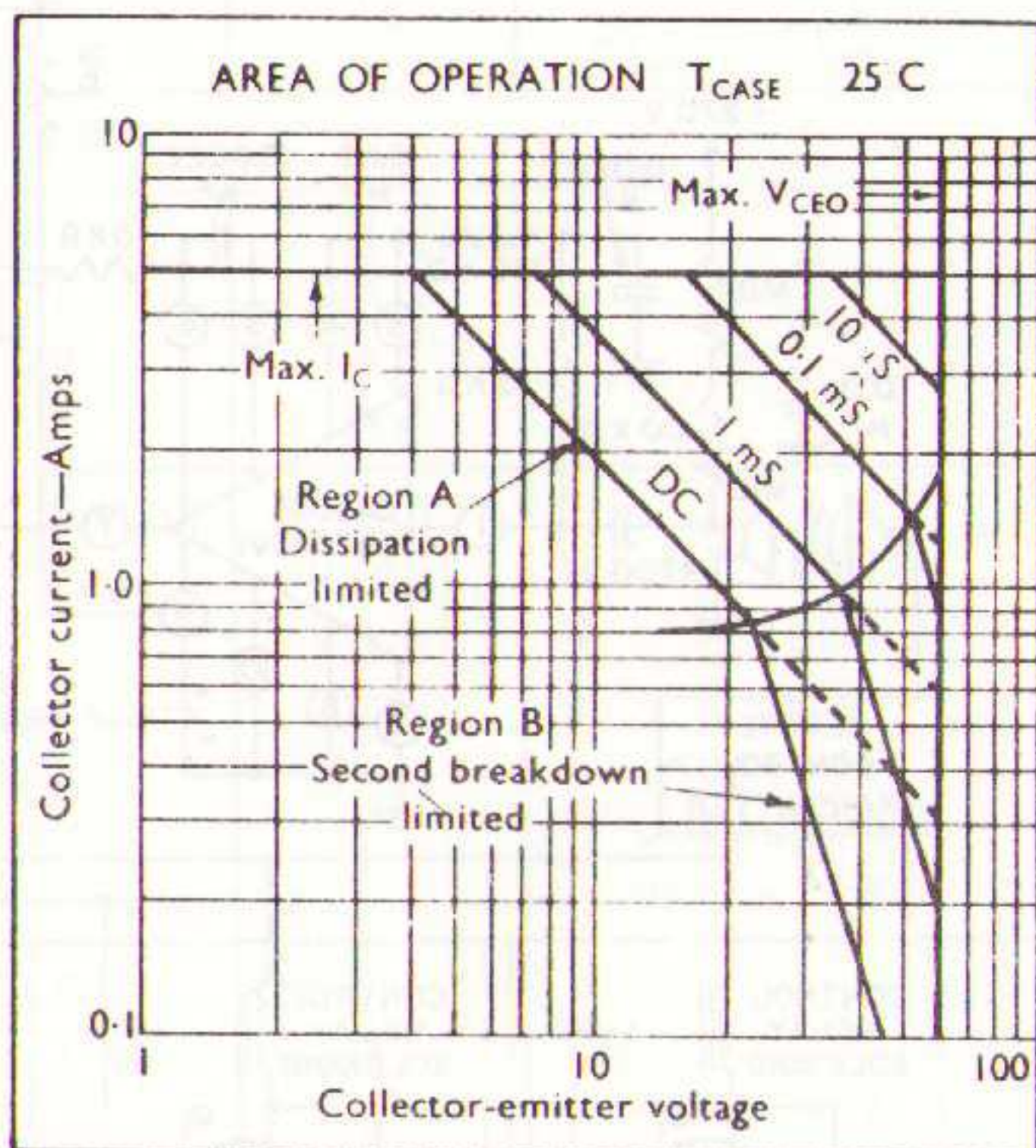


Fig. 7

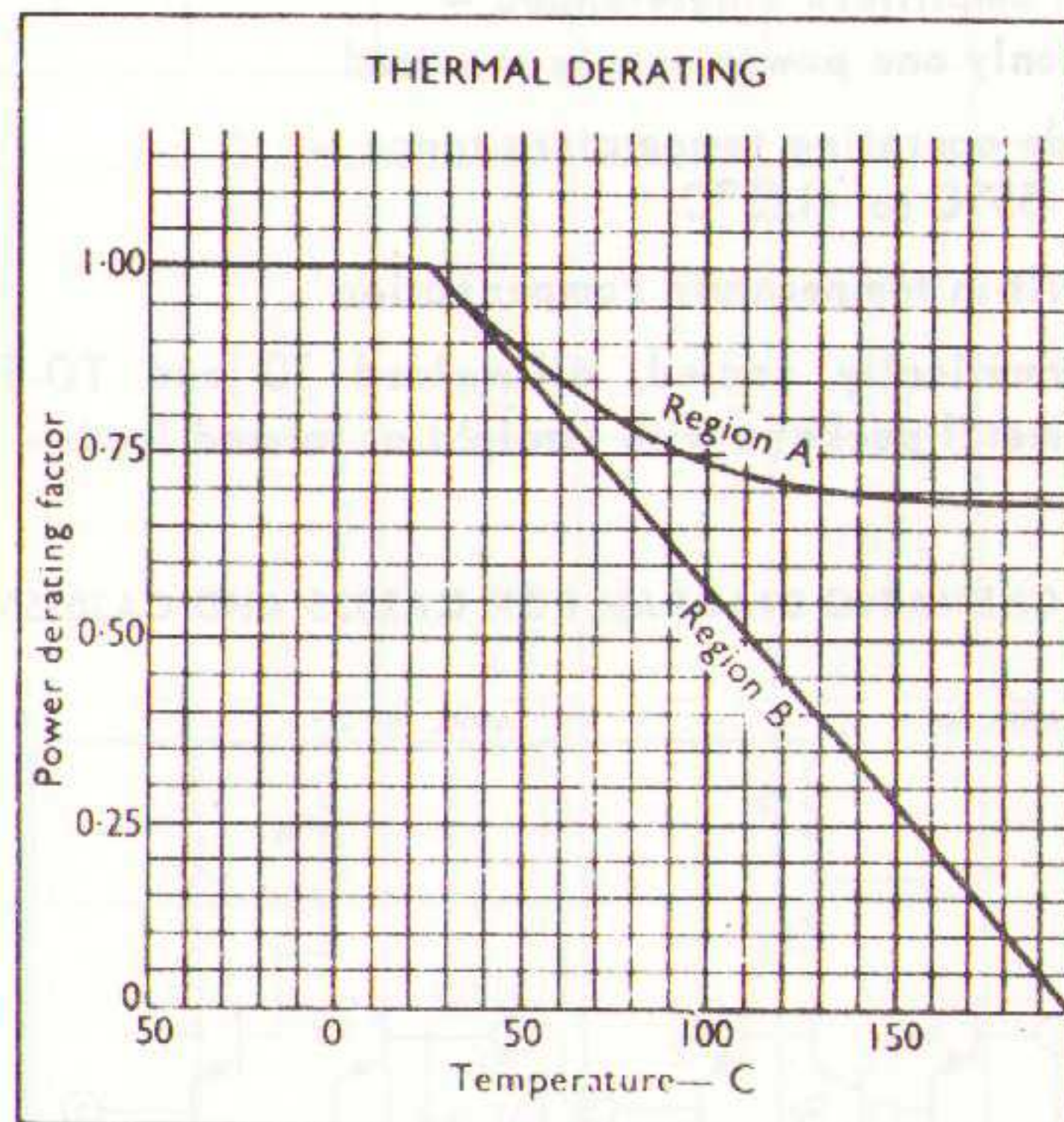


Fig. 8

In region A the device must be derated for high case temperatures in the normal manner, since junction temperature is a function of thermal resistance and thermal time constants only. However, the second breakdown locus only varies slightly with case temperature and a separate (less severe) derating may be applied to region B as shown in Fig. 8. In practice, the reduced derating curve for area B may not be available so the same derating as area A may be applied and will always be conservative.

Note that the intersection of areas A and B will vary with temperature and that the worst case must always be taken. The dotted lines on Fig. 7 give the dissipation limited area for derating purposes.

References

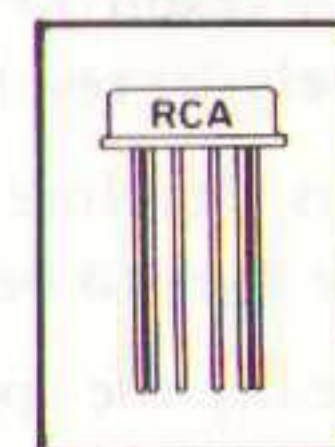
- 1 F. Bergmann and D. Gerstner, 'Thermisch bedingte Stromeinschnürung bei Hochfrequenz-Leistungstransistoren'. Arch.elekt.Übertr., Vol. 17, pp. 467-475, Oct. 1963.
- 2 IEEE Transactions on Electron Devices—Special Issue on Second Breakdown (1) August/September 1966. Volume ED-13, Number 8/9.
- 3 IEEE Transactions on Electron Devices—Special Issue on Second Breakdown (2) October, November 1966.

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

HIGHLIGHTS

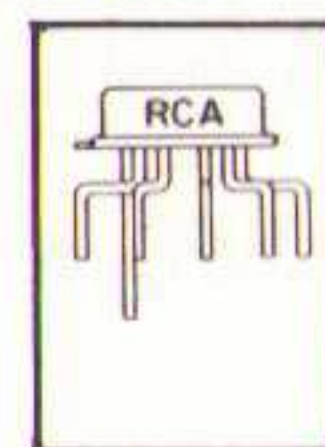
- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to $+125^{\circ}\text{C}$
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

CA3035



10-LEAD
TO-5

CA3035V1



FORMED-LEAD
10-LEAD TO-5

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

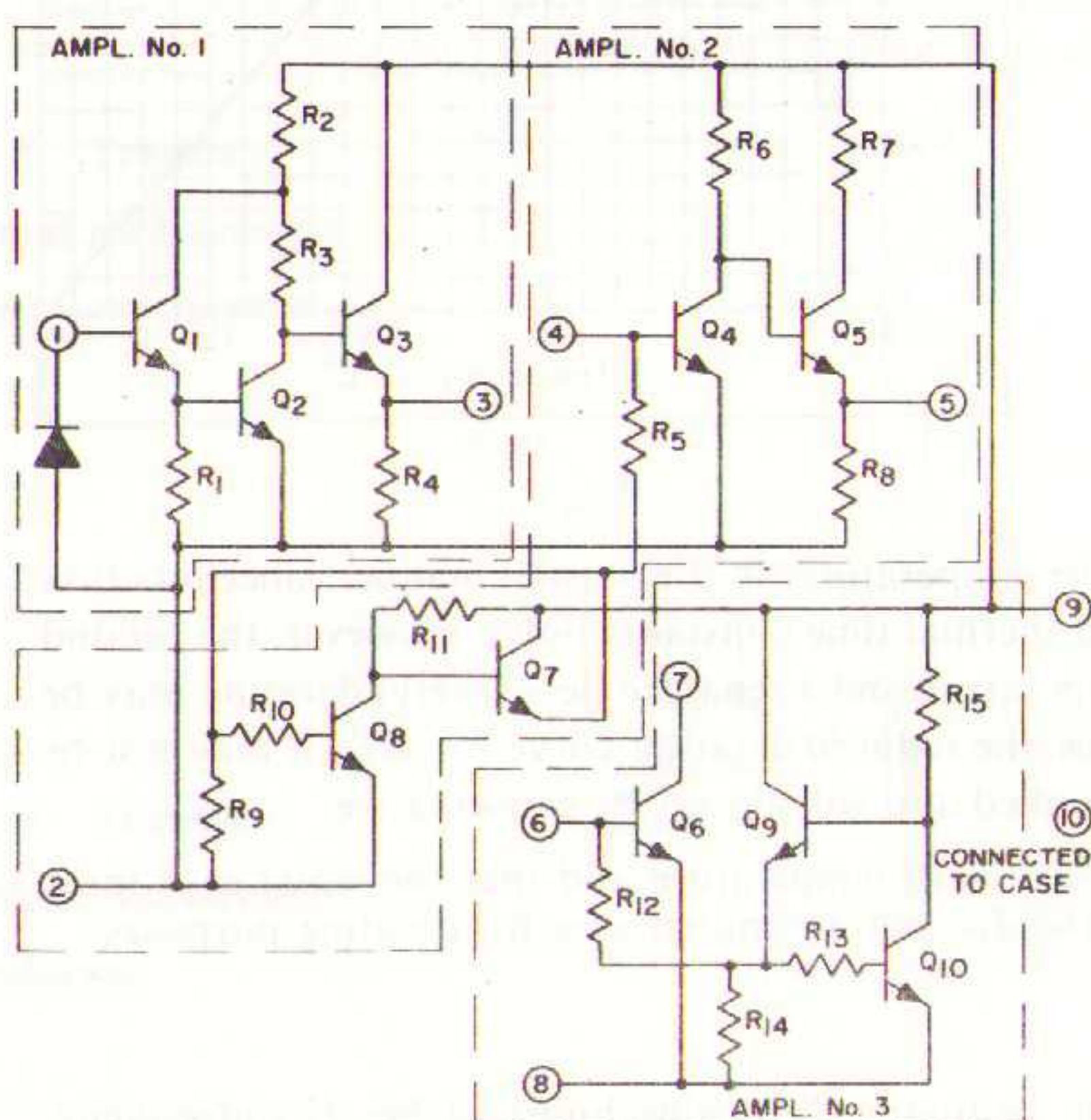


Fig. 1

TYPICAL REMOTE CONTROL SYSTEM

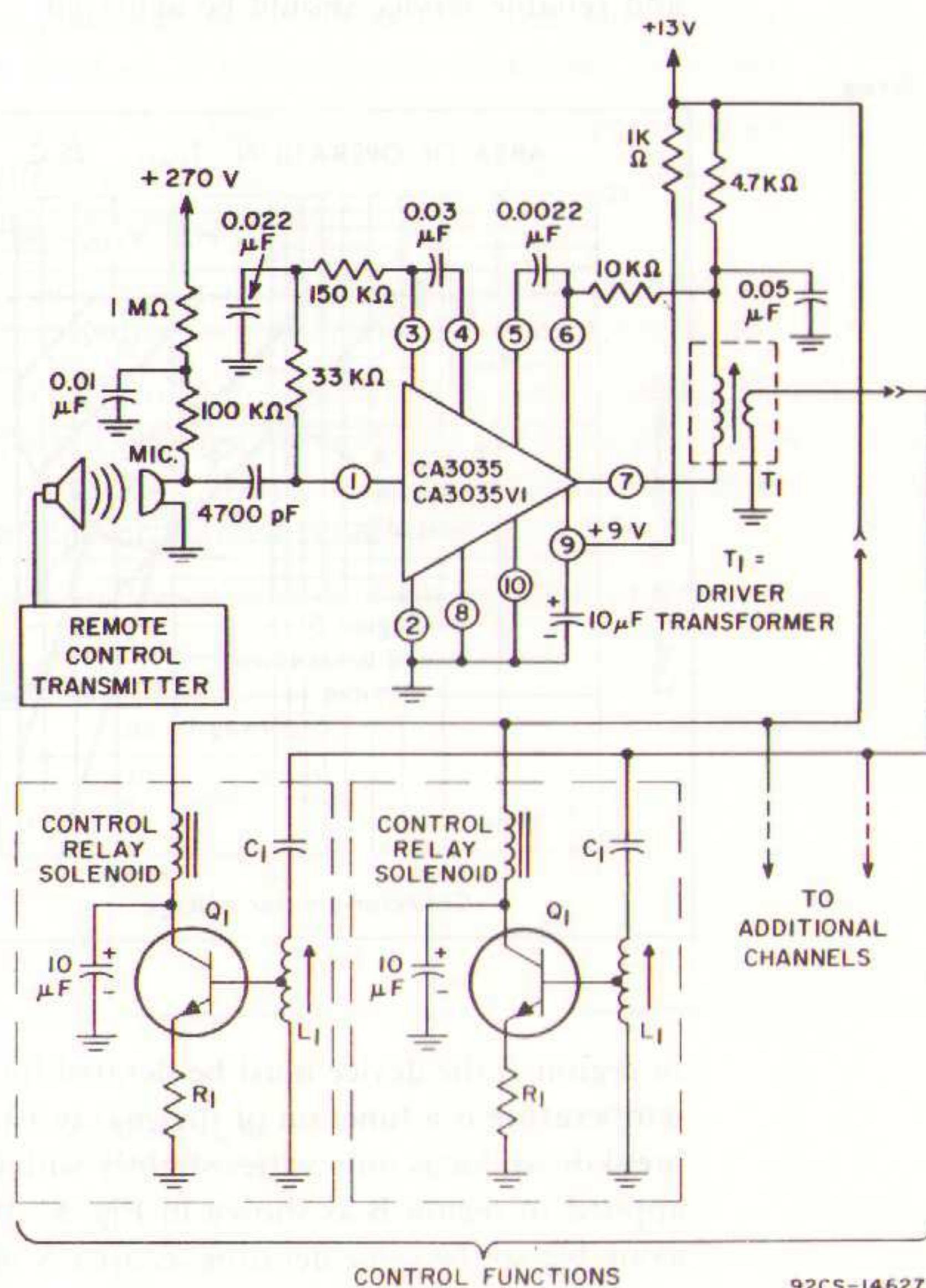


Fig. 2

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Printed in U.S.A.
CA3035, CA3035V1 6-67

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range -55°C to +125°C

Storage Temperature Range -65°C to +200°C

Device Dissipation 300 mW

Input Voltage 1 V p-p

Supply Voltage +15V

ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARAC-TERISTICS CURVES	LIMITS			UNITS
				CA3035, CA3035V1			
				Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3	VCC = +9V	Fig.3	-	2	-	V
	V5			-	1.9	-	V
	V7			-	4.9	-	V
Total Current Drain	Id	VCC = +9V, RL3 = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain:							
Amplifier No.1	A1	f = 40 kHz, VCC = +9V		40	44	-	dB
Amplifier No.2	A2			40	46	-	dB
Amplifier No.3	A3			38	42	-	dB
Output Voltage Swing	Vout	RL1 = 10KΩ RL2 = 10KΩ RL3 = 5KΩ Sinusoidal Output, VCC = +9V		-	2	-	Vp-p
	V1out			-	2.6	-	Vp-p
	V2out			-	8	-	Vp-p
	V3out			-		-	
Input Resistance:							
	Amplifier No.1	R1in	f = 40 kHz	-	50K	-	Ω
	Amplifier No.2	R2in		-	2K	-	Ω
	Amplifier No.3	R3in		-	670	-	Ω
Output Resistance	R1out	f = 40 kHz		-	270	-	Ω
	R2out			-	170	-	Ω
	R3out			-	100K	-	Ω
Bandwidth at -3dB point:							
	Amplifier No.1	BW1	Fig.5	-	500	-	kHz
	Amplifier No.2	BW2	Fig.6	-	2.5	-	MHz
	Amplifier No.3	BW3	Fig.7	-	2.5	-	MHz
Noise Figure							
Amplifier No.1	NF1	f = 1 kHz, RS = 1 KΩ	Fig.4	-	6	7	dB
Sensitivity		VCC = +13 V Relay (K1) Current = 7.5 mA	Fig.2	-	100	150	μV

STATIC CHARACTERISTICS

TEST CIRCUIT

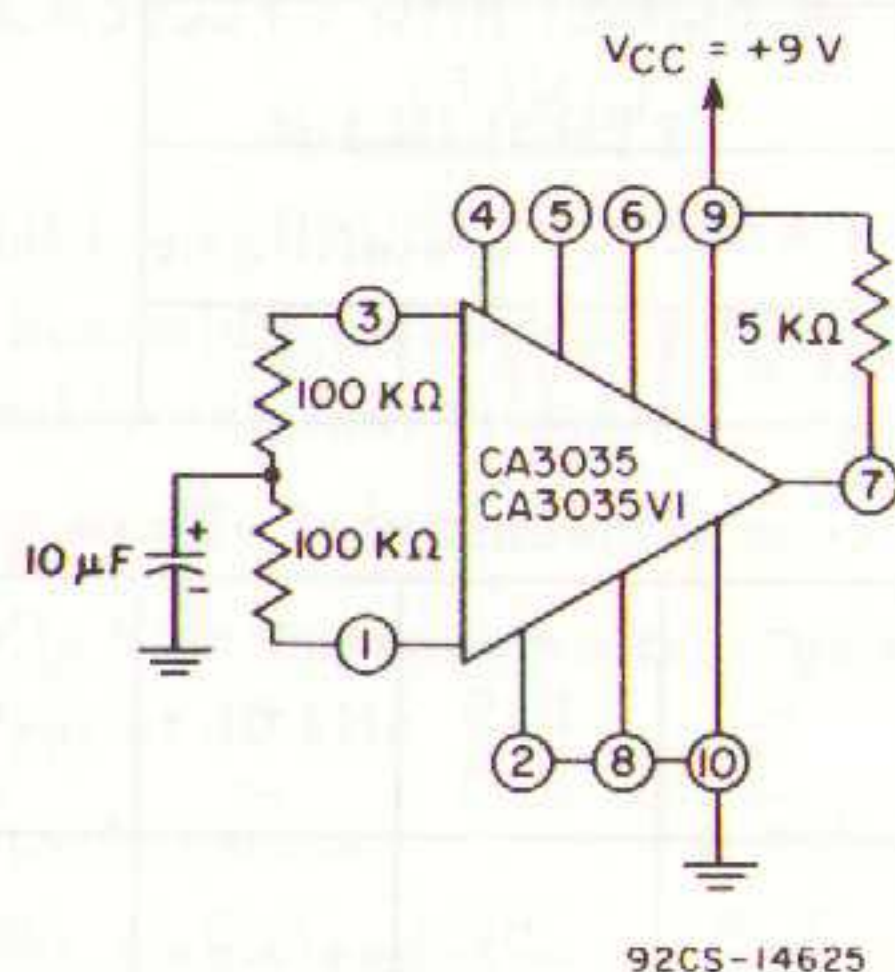


Fig. 3

NOISE FIGURE TEST CIRCUIT

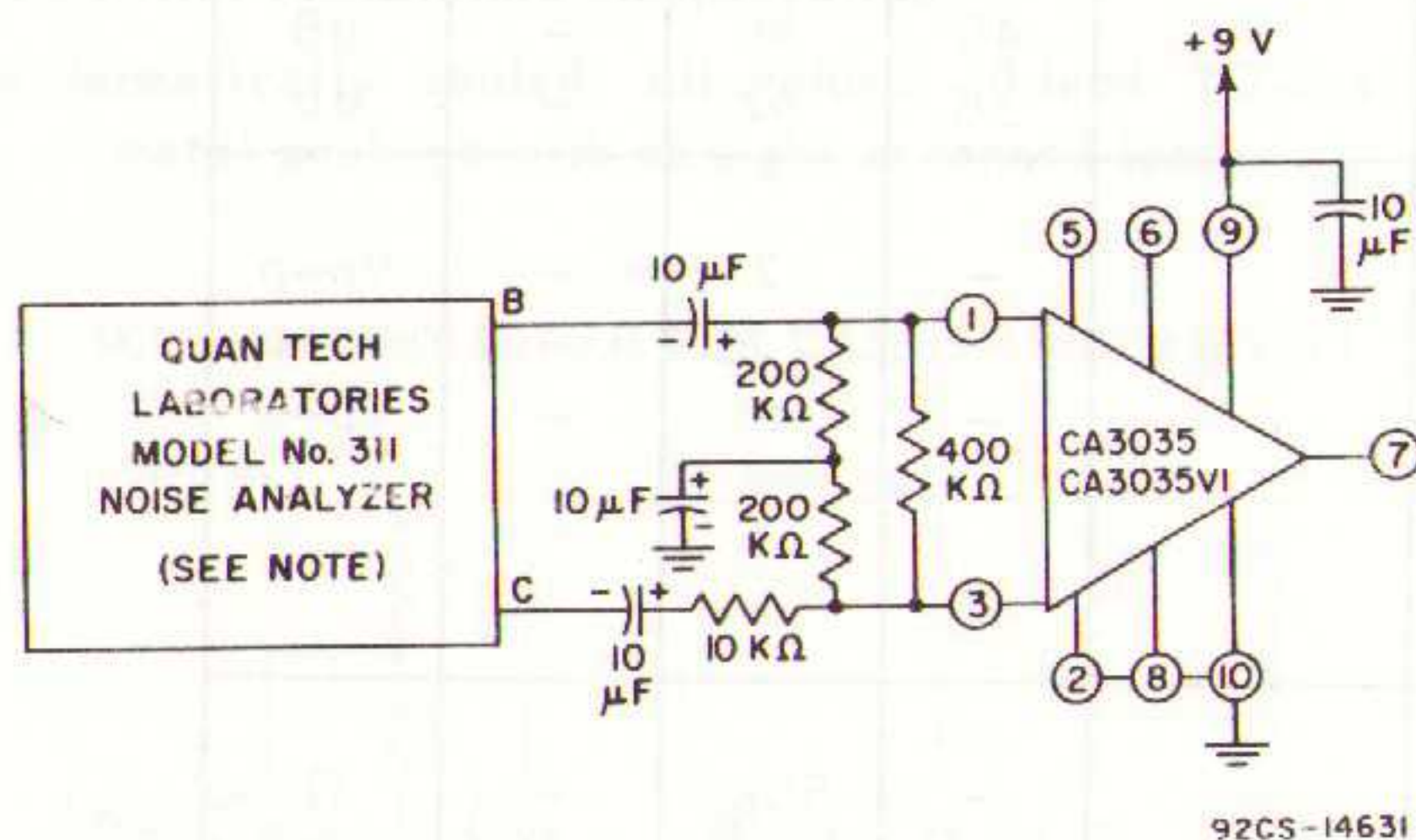
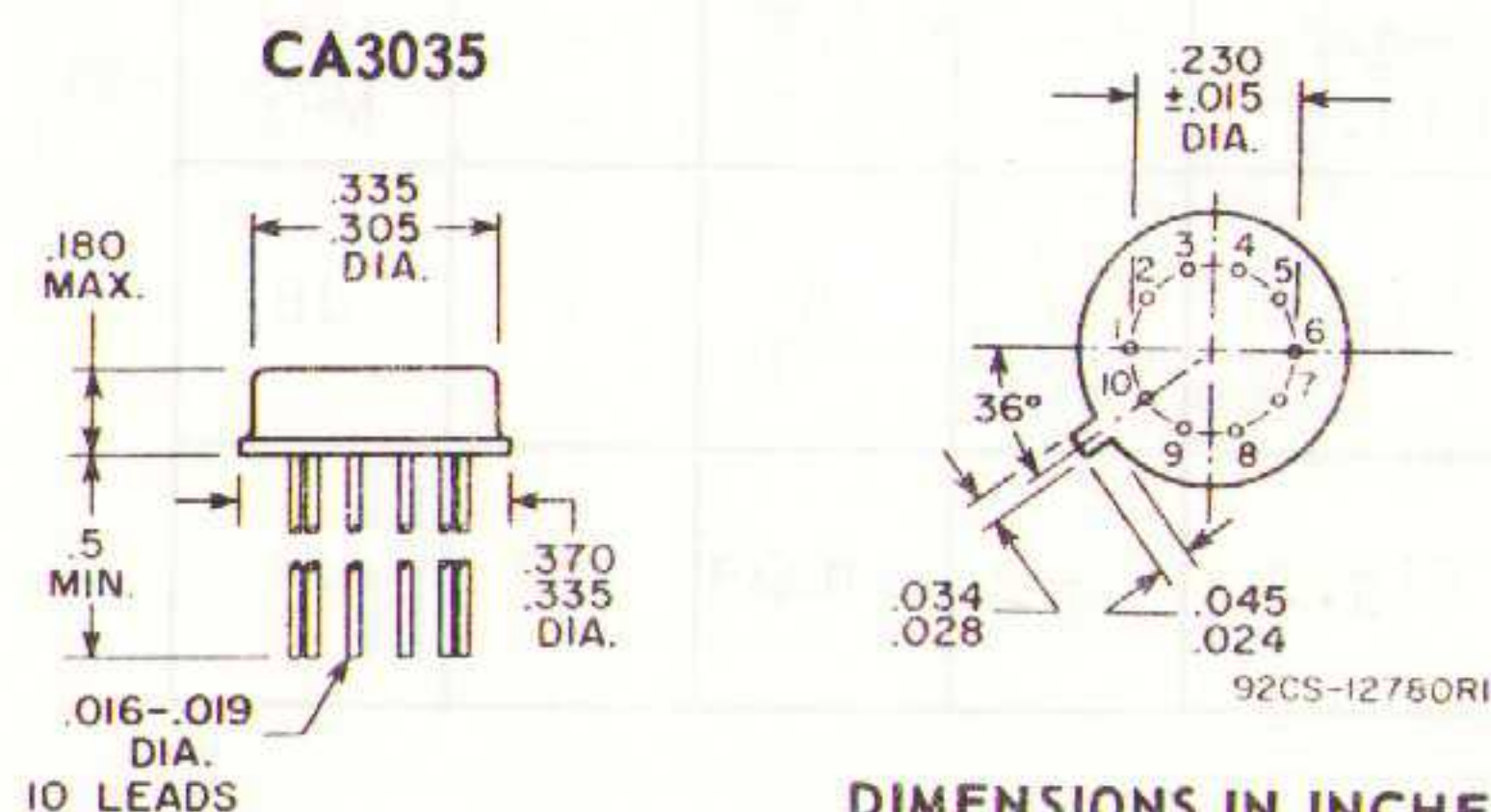


Fig. 4

NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

DIMENSIONAL OUTLINES



DIMENSIONS IN INCHES

TYPICAL 1st-AMPLIFIER RESPONSE

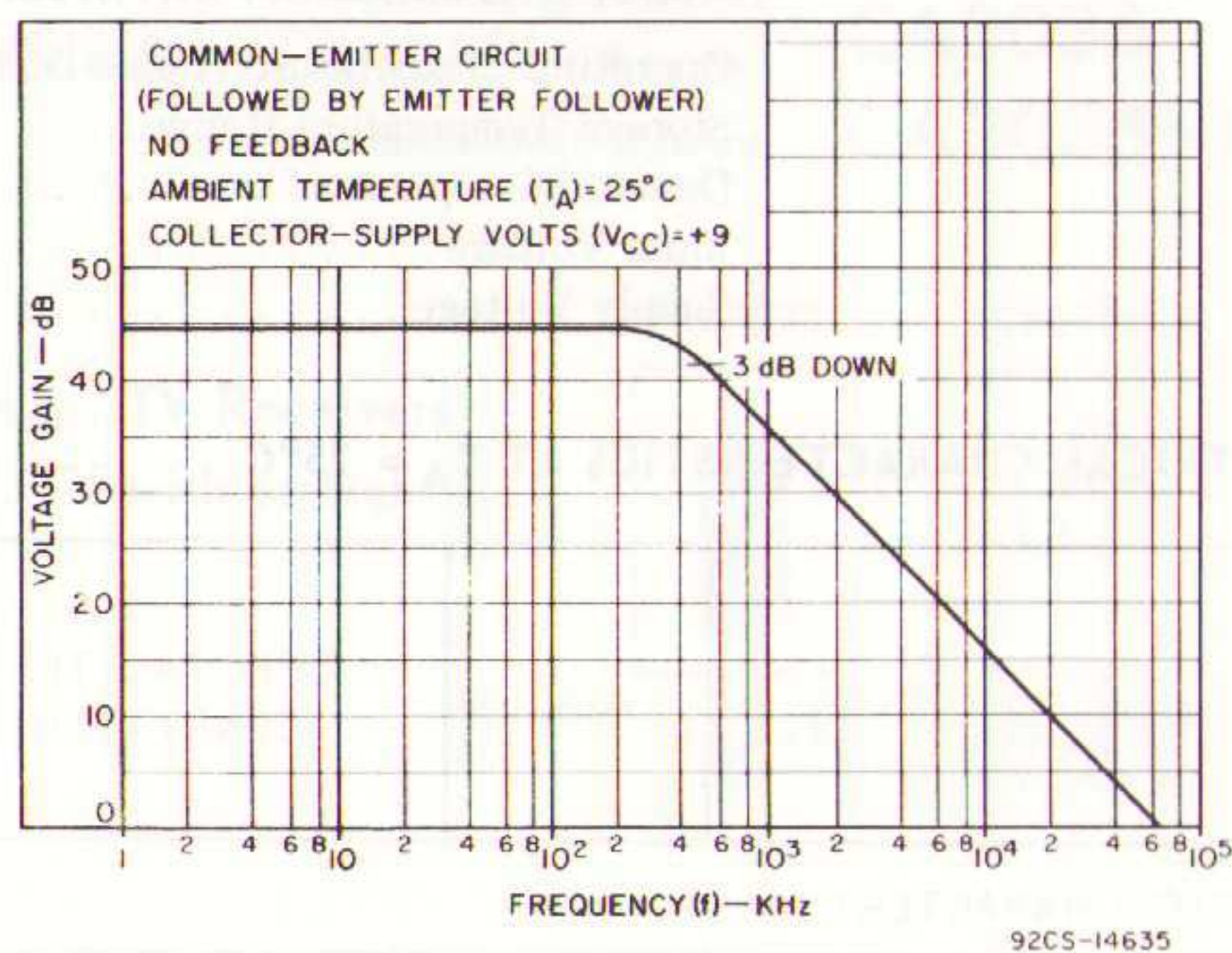


Fig. 5

TYPICAL 2nd-AMPLIFIER RESPONSE

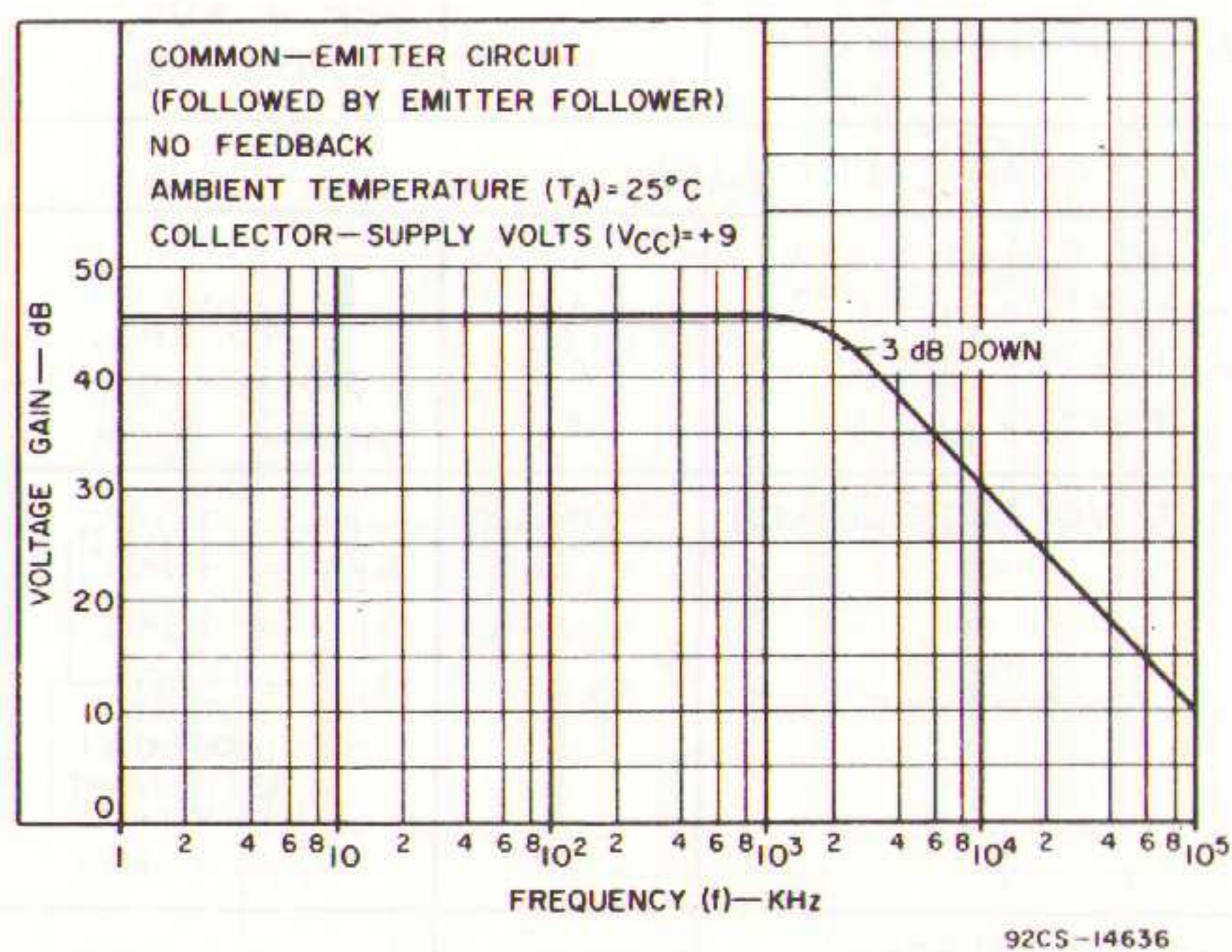


Fig. 6

TYPICAL 3rd-AMPLIFIER RESPONSE

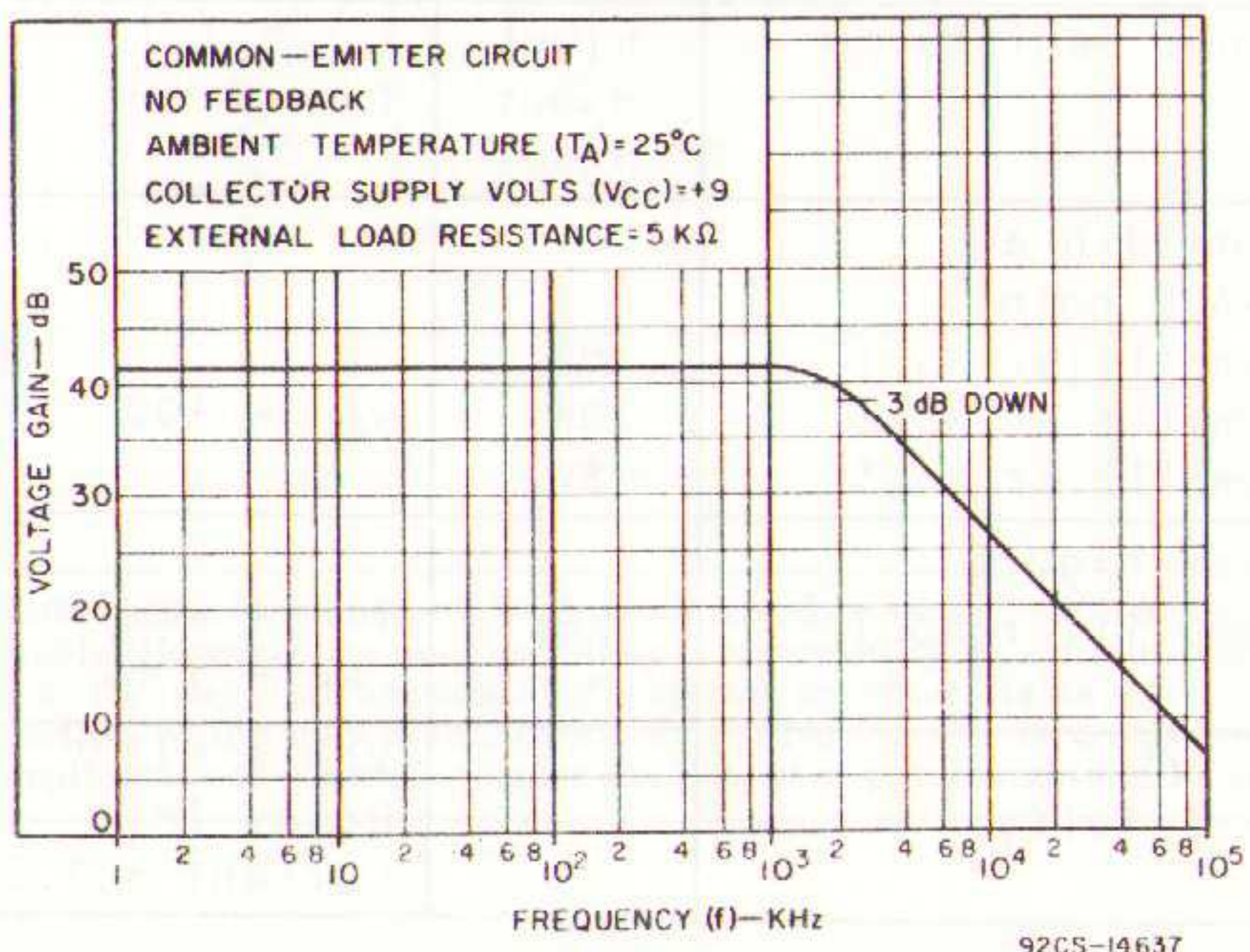


Fig. 7

Onze activiteiten breiden zich steeds verder uit. Ons personeelsbestand (nu reeds 8 man) moet echter meegroeien. Daarom zoeken wij contact met serieus geïnteresseerden voor een gevarieerde functie in ons snelgroeiend dynamisch bedrijf. Niet alleen voor direct, doch ook voor in de toekomst beschikbare functies, want wij zijn van plan te blijven groeien

BENT U

- tussen 18 en 24 jaar, in militaire dienst geweest en goed thuis in de hedendaagse technieken, zoals halfgeleiders, digitale techniek, audio, vermogensregelingen, analoge techniek, MOS-techniek, procesautomatisering, enz., enz. en bereid, u ten volle voor uw taak in te zetten, dan bent u wellicht bij ons op uw plaats.

WIJ BIEDEN U

- geen "werk in een hokje", doch een veel omvattende technisch-commerciële functie, waarbij alle mogelijke werkzaamheden tot uw taak kunnen behoren. Dit betekent, dat u het ene ogenblik een cliënt uit een technisch probleem helpt, terwijl u het volgende moment wellicht onze orderadministratie assisteert bij het verzendklaar maken van een order, of een ingewikkeld besturingssysteem voor één onze relaties uitknobbelt of een nieuw onderdelenpakket ontwikkelt. Wellicht vertoont deze functie overeenkomst met uw hobbiaanse aspiraties, waardoor deze functie dubbel interessant voor u is?

Mocht u geïnteresseerd zijn of nadere gegevens willen over de mogelijkheden, stuurt u dan uw sollicitatie aan ons adres:

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Van Dam Elektronica
afdeling: personeelszaken
Postbus 3149 te Rotterdam-noord

RCA-CA3047 is a high performance integrated circuit operational amplifier consisting of two differential amplifiers in cascade and a single-ended class-B power output stage on a single monolithic silicon chip. This device features high input impedance, high gain, high power output, and low input-offset voltage and current.

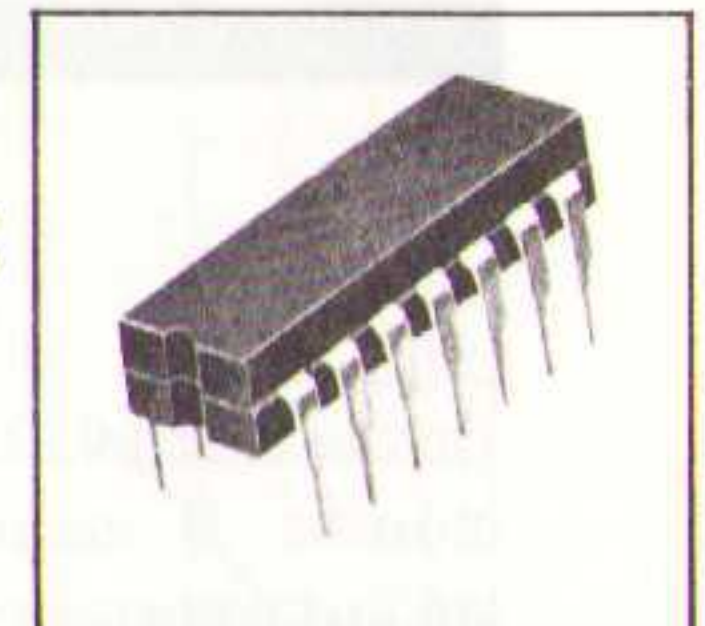
RCA-CA3047 is supplied in an easy-to-insert "dual-in-line" plastic package for applications requiring high packing densities.

FEATURES

- High Open-Loop Differential Gain 90 dB typ
- High Power Output Capability 122 mW typ
- Large Output Voltage Swing 22 Vp-p typ
- Very Low Input Offset Current 5 nA typ
- Low Input Bias Current 83 nA typ
- High Input Impedance 1.5 MΩ typ
- Exceptionally High Common-Mode Rejection Ratio 100 dB typ

OPERATIONAL AMPLIFIER

Two Differential Amplifiers in Cascade Plus One Single-Ended Class B Power Output Stage

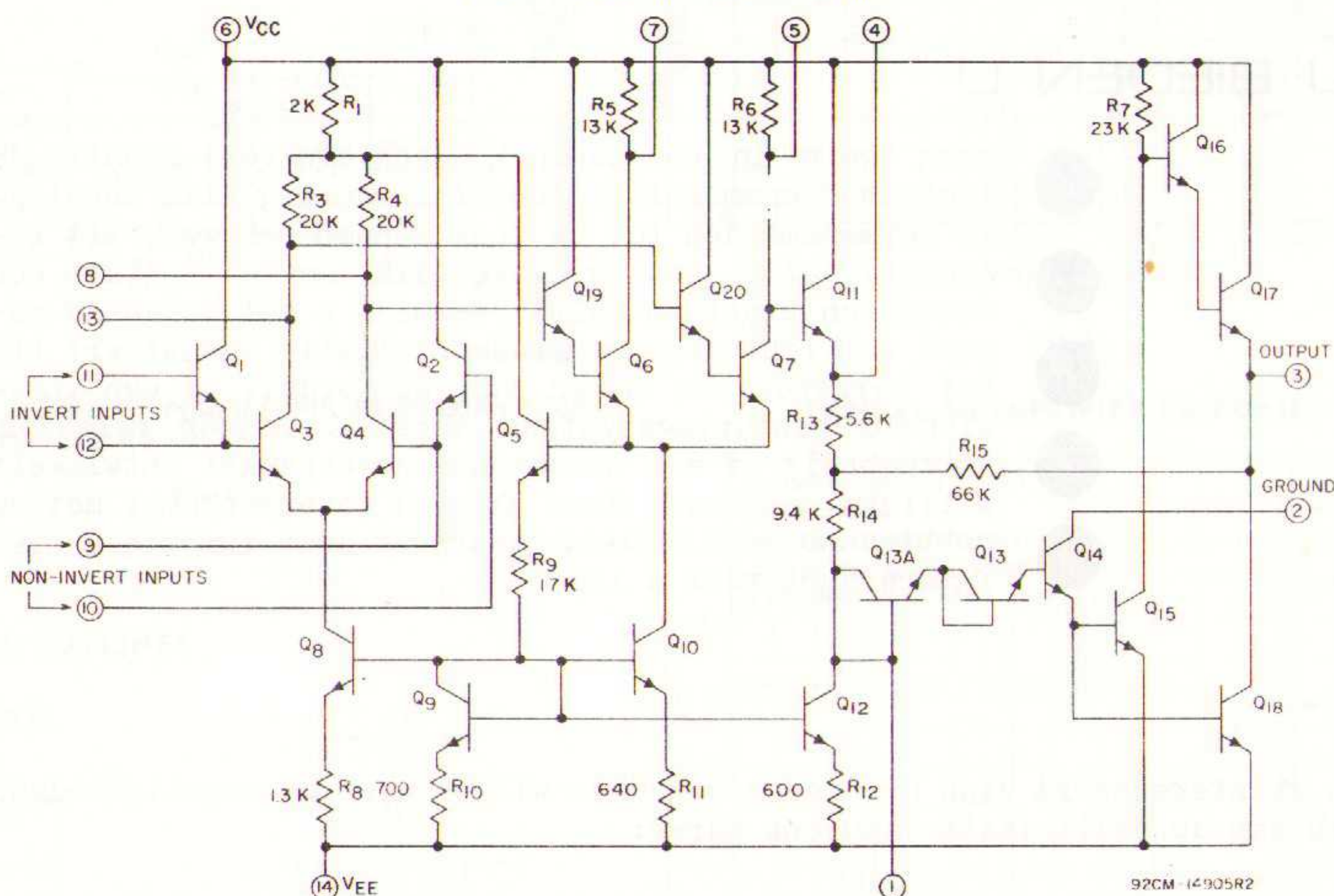


JEDEC TO-116
PLASTIC PACKAGE

APPLICATIONS

- Comparator
- Electrometer
- Audio Amplifier
- Power Amplifier
- Operational Functions
- Servo Driver
- DC & Video Amplifiers
- Multivibrator
- Oscillator
- Narrow Band and Band Pass Amplifiers
- Companion Application Note, ICAN-5641 "Application of RCA CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers."

FIG.1 - SCHEMATIC DIAGRAM



The resistance values included on the schematic diagrams have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as $\pm 30\%$.

RCA reserves the right to make any changes in the Resistance values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS

OPERATING AMBIENT TEMPERATURE RANGE 0°C to +70°C

STORAGE AMBIENT TEMPERATURE RANGE -25°C to +85°C

MAXIMUM INPUT-SIGNAL VOLTAGE[●] ± 10 VMAXIMUM DEVICE DISSIPATION:[▲]

At Ambient { up to 25°C 750 mW
 Temperatures { above 25°C Derate at 6.67 mW/°C

Absolute-Maximum Voltage and Current Limits at T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS*	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	12 V	50 mA	6 14 2 & 10	+12 -12 ground
2	12 V	14 V	6 14 10	+12 -12 ground
3	50 mA	50 mA	6 14 2 & 10	+12 -12 ground
4	20 mA	1 V	6 14 2 & 10	+12 -12 ground
5	0	12 V	6 14 2 & 10	+12 -12 ground
6	0	14 V	14 2 & 10	-12 ground
7	0	12 V	6 14 2 & 10	+12 -12 ground
8	0	12 V	6 14 2 & 10	+12 -12 ground

TERMINAL	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS*	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
9	10 V	10 V 10 mA	6 14 2 & 10	+12 -12 ground
10	10 V	10 V 10 mA	6 14 2	+12 -12 ground
11	10 V	10 V 10 mA	6 14 2 & 10	+12 -12 ground
12	10 V	10 V 10 mA	6 14 2 & 10	+12 -12 ground
13	0	12 V	6 14 2 & 10	+12 -12 ground
14	14 V	0	6 2 & 10	+12 ground
CASE	INTERNALLY CONNECTED TO TERMINAL No.14 DO NOT GROUND			

● Under no circumstances should current exceed 10 mA. See voltage and current limits for Terminals 9 through 12.

▲ Maximum dissipation capability of 14-lead plastic dual in-line package.

* 1 MΩ between terminals No.11 and 3, 1 μF from terminal No.13 to ground and 1 μF from terminal No.13 to ground and 1 μF from terminal No.8 to ground.

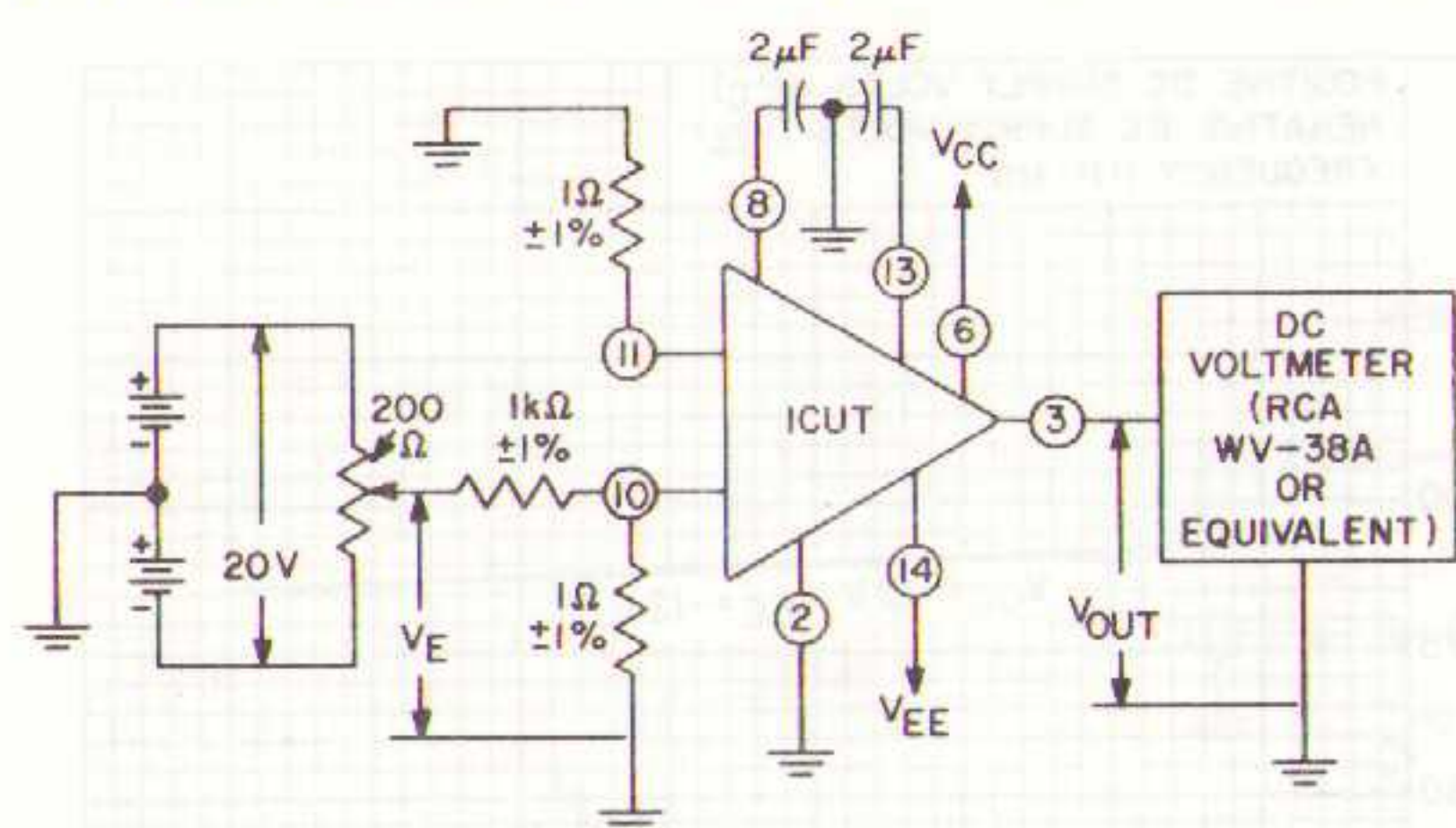
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ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$, $V_{CC} = +12\text{V}$, $V_{EE} = -12\text{V}$

Characteristics	Symbols	Test Circuits	Special Test Conditions	Limits			Units	Typical Characteristics Curves
		Fig.		CA3047				Fig.
				Min.	Typ.	Max.		
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}	2		-	2.6	5	mV	2A
Input Offset Current	I_{IO}	3		-	5	35	nA	3A
Input Bias Current	I_I	3		-	83	350	nA	3B
Input Offset Voltage Drift -55°C to 125°C	$V_{IO}/\Delta T$	2		-	6.6	-	$\mu V/^{\circ}C$	2A
Input Offset Current Drift -55°C to 25°C 25°C to 125°C	$I_{IO}/\Delta T$	3		-	1	-	$nA/^{\circ}C$	3A
				-	.08	-	$nA/^{\circ}C$	
Input Offset Voltage Sensitivity:								
Positive	$\Delta V_{IO}/\Delta V_{CC}$	2		-	0.3	0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	2		-	0.3	0.5	mV/V	none
Device Dissipation	P_T	2		60	120	180	mW	none
DYNAMIC CHARACTERISTICS: f = 1 kHz for all but BW								
Open-Loop Differential Voltage Gain	A_{OL}	4		84	90	-	dB	4A 4B
60 dB-Amplifier Bandwidth at -3 dB Point	BW	4C	$C_X, C_Y = 0.001 \mu F$	-	230	-	kHz	4B
Common-Mode Rejection Ratio	CMR	5		84	100	-	dB	5A
Common-Mode Input-Voltage Range	V_{CMR}	5		-7.5	+5,-9	+3.5	V	none
Maximum Output-Voltage Swing	$V_{O(P-P)}$	4	$R_L = 500 \Omega$	18	22	-	V_{P-P}	none
Input Impedance	Z_{in}	6		0.15	1.5	-	$M\Omega$	none
Output Current	I_o	4	$R_L = 500 \Omega$	36	44	-	mA(P-P)	4D
Slew Rate	SR	none		-	1.2	-	V/ μs	none
Power Output (THD 10%)	P_o	4	$R_L = 500 \Omega$ $C_X, C_Y = 0.001 \mu F$	80	122	-	mW	4E

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FIG.2 - INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT



Procedure:

92CS-14895

INPUT OFFSET VOLTAGE

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

INPUT OFFSET VOLTAGE SENSITIVITY

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase V_{CC} by 1 volt and record output voltage (V_{OUT}).
3. Decrease V_{CC} by 1 volt and record output voltage (V_{OUT}).
4. Divide the difference between V_{OUT} measured in steps 2 and 3 by change in V_{CC} in steps 2 and 3

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}(\text{step 2}) - V_{OUT}(\text{step 3})}{2 \text{ volts}}$$

5. Refer the reading to the input by dividing by the Open Loop Voltage Gain (A_{OL}).

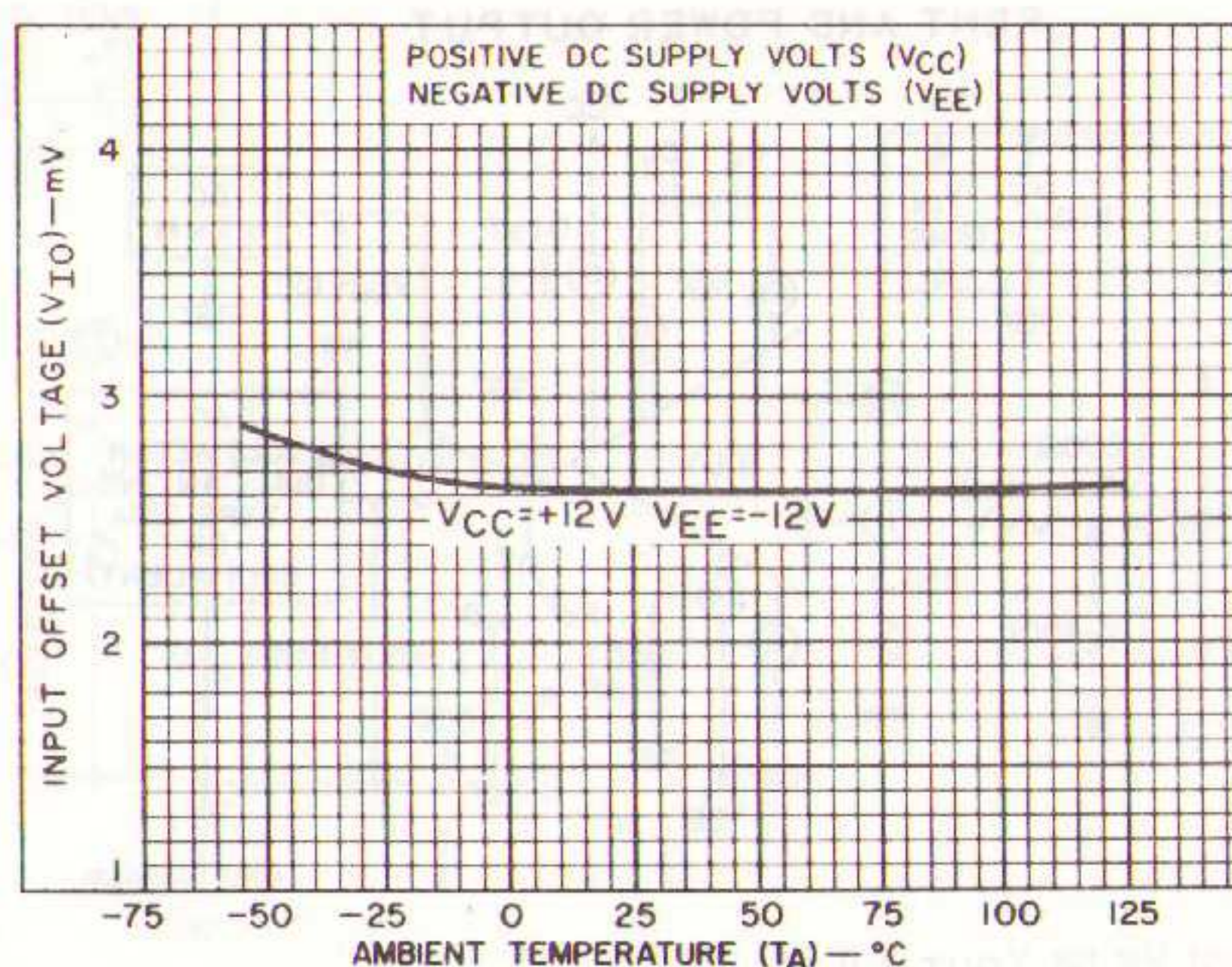
$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$$P_T = V_{CC}I_C + V_{EE}I_E$$

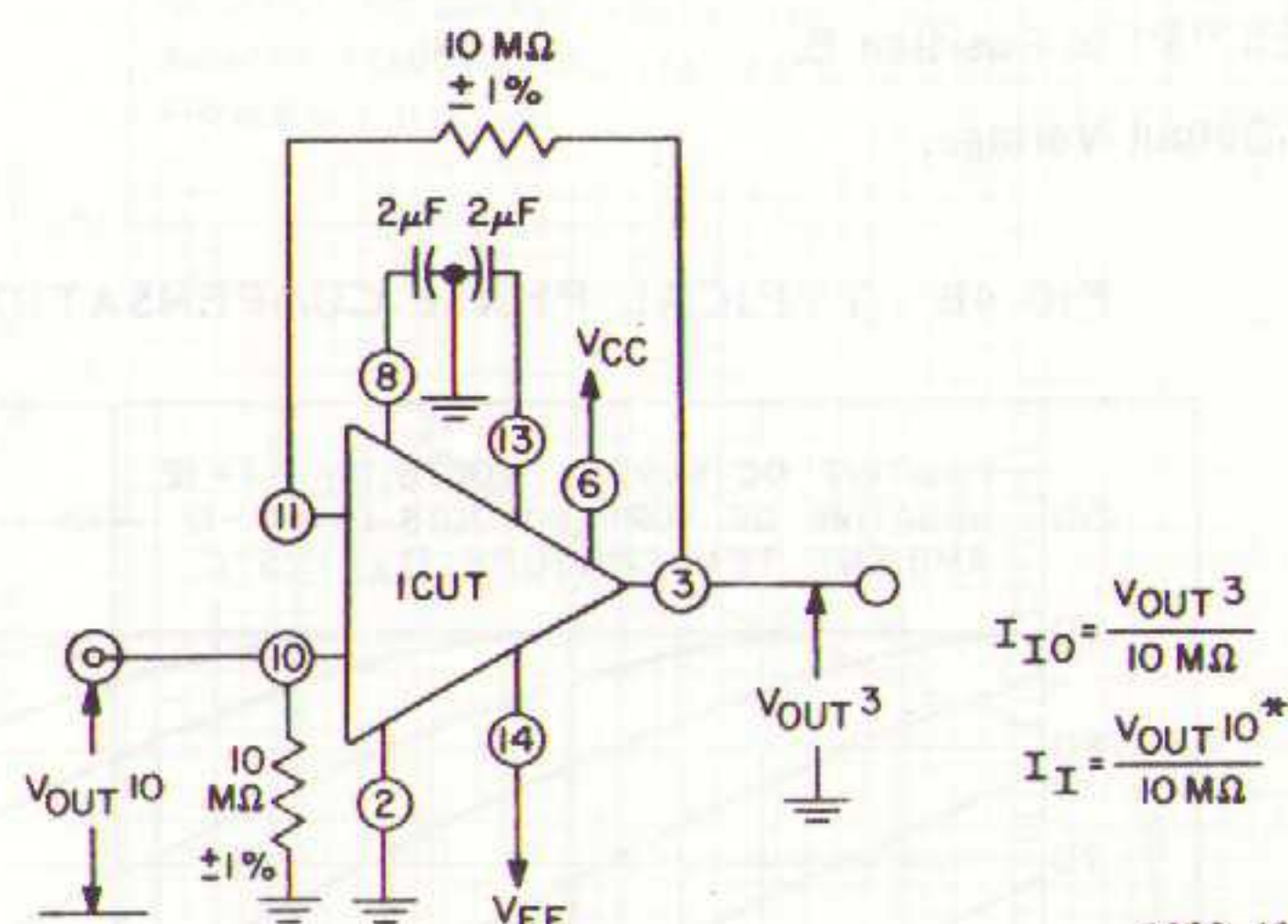
 I_C = Direct Current into Terminal No.6. I_E = Direct Current out of Terminal No.14.

FIG.2A - TYPICAL INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



92CS-15287

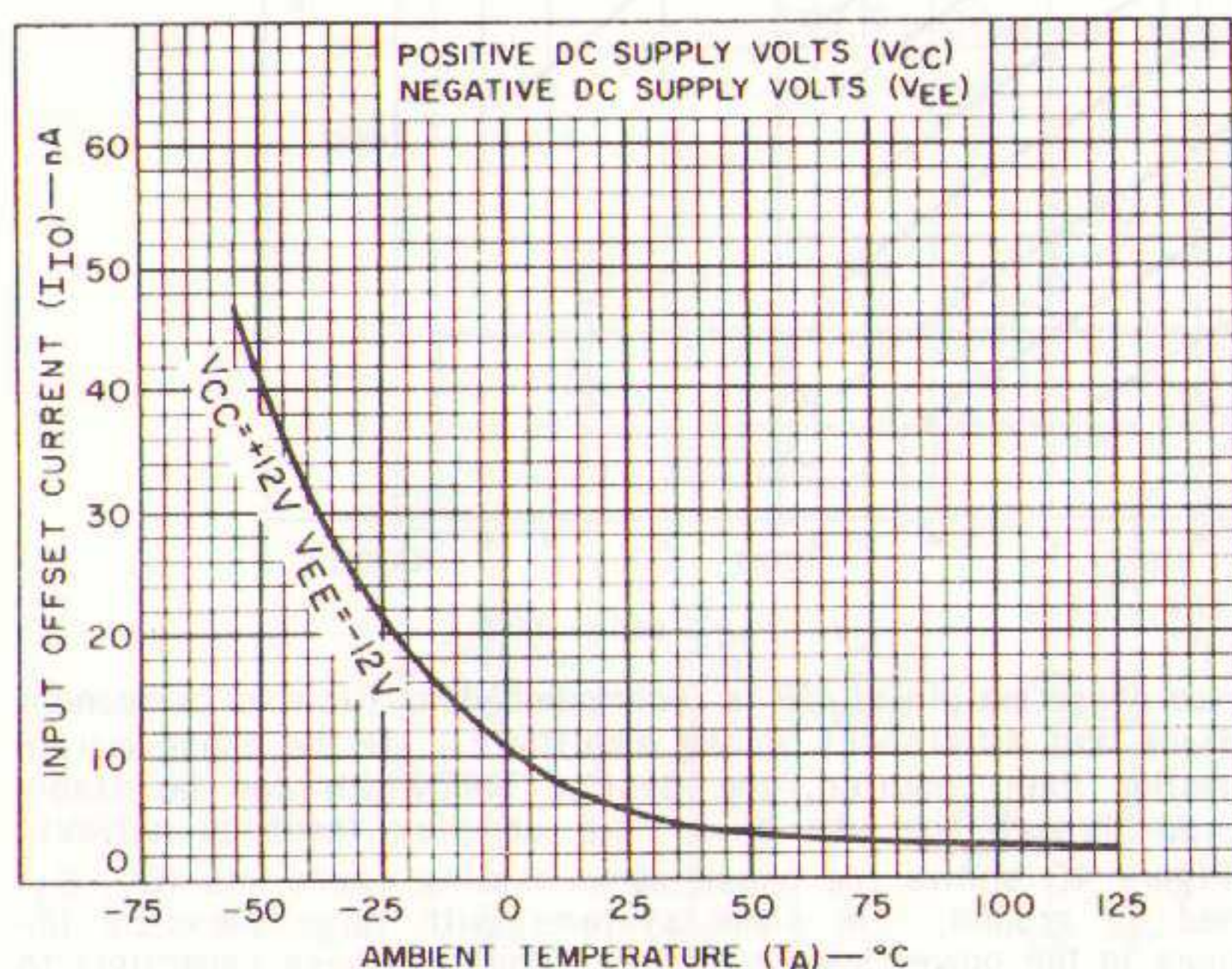
FIG.3 - INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT



92CS-14894

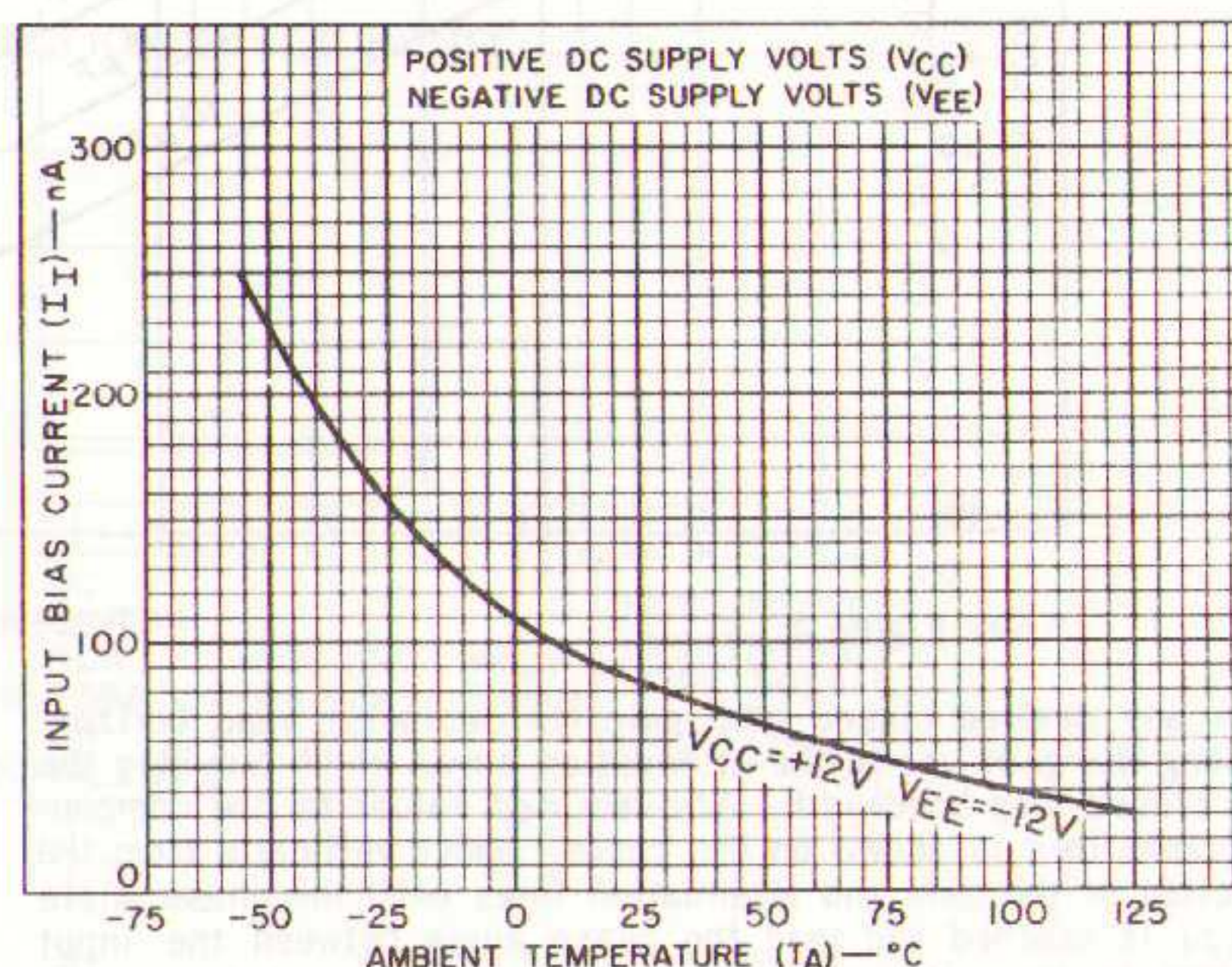
* This measurement must be made with a differential voltmeter that provides extremely high input resistance at null.

FIG.3A - TYPICAL INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



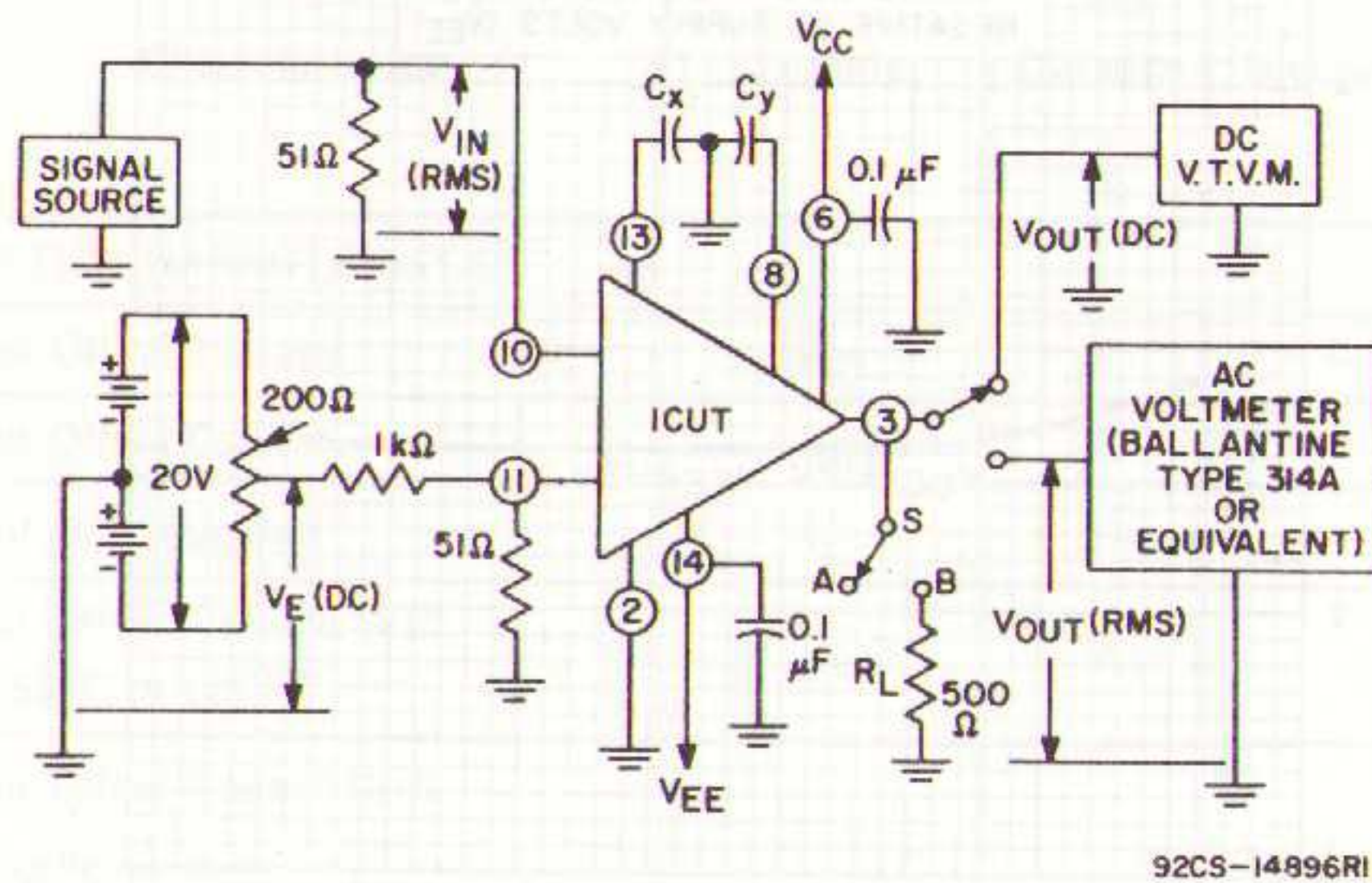
92CS-15288

FIG.3B - TYPICAL INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



92CS-15289

FIG.4 - OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, OUTPUT CURRENT AND POWER OUTPUT

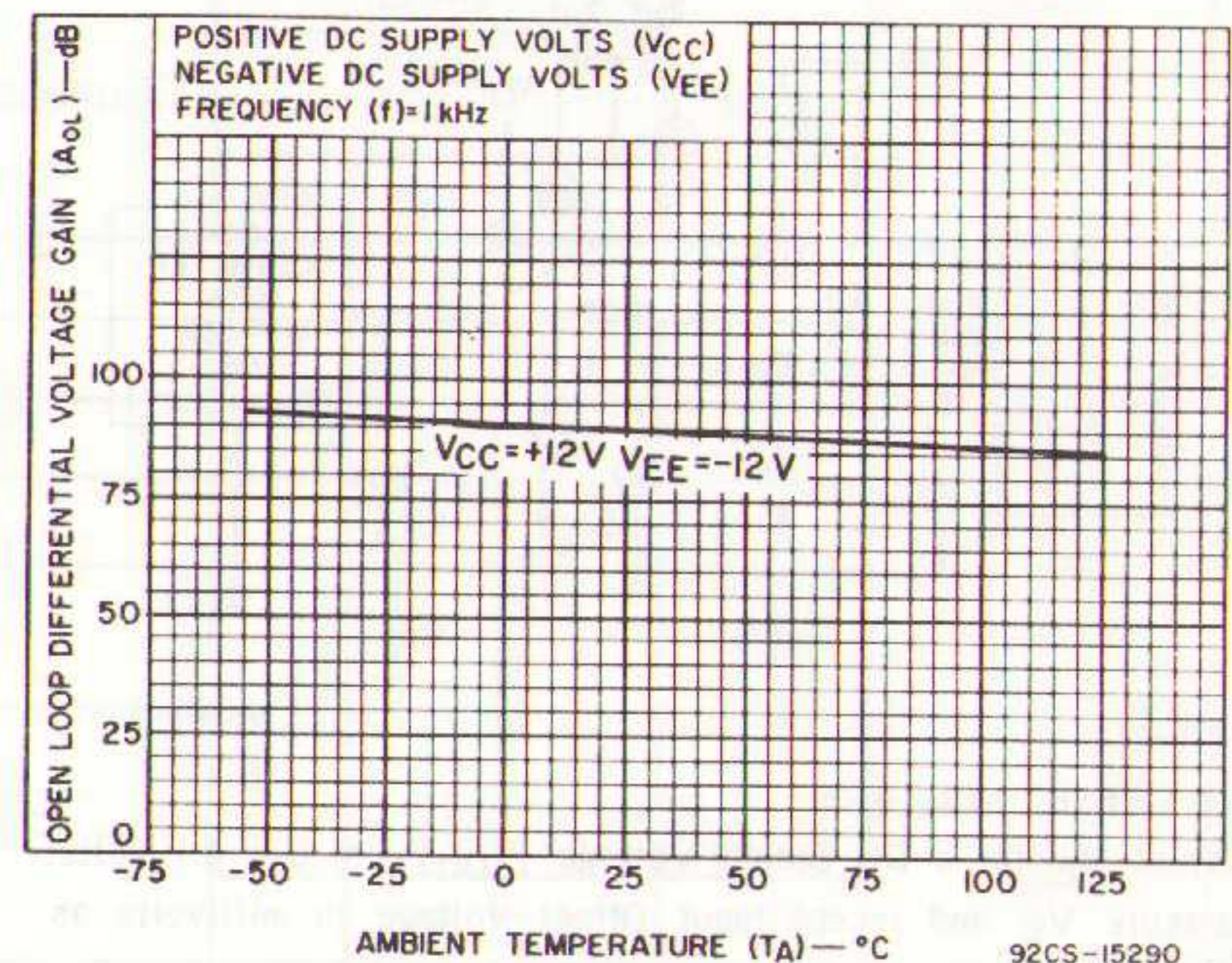


1. Adjust V_E for $V_{OUT} = 0 \pm 0.1$ V DC.
2. Set Switch "S" to Position A.
3. Measure Open-Loop Differential Voltage Gain (A_{OL}) at $f = 1$ kHz.

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

4. Measure Maximum Peak-to-Peak Output Voltage at $f = 1$ kHz.
5. Set Switch "S" to Position B.
6. Measure Output Voltage.

FIG.4A - TYPICAL OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN VS. AMBIENT TEMPERATURE

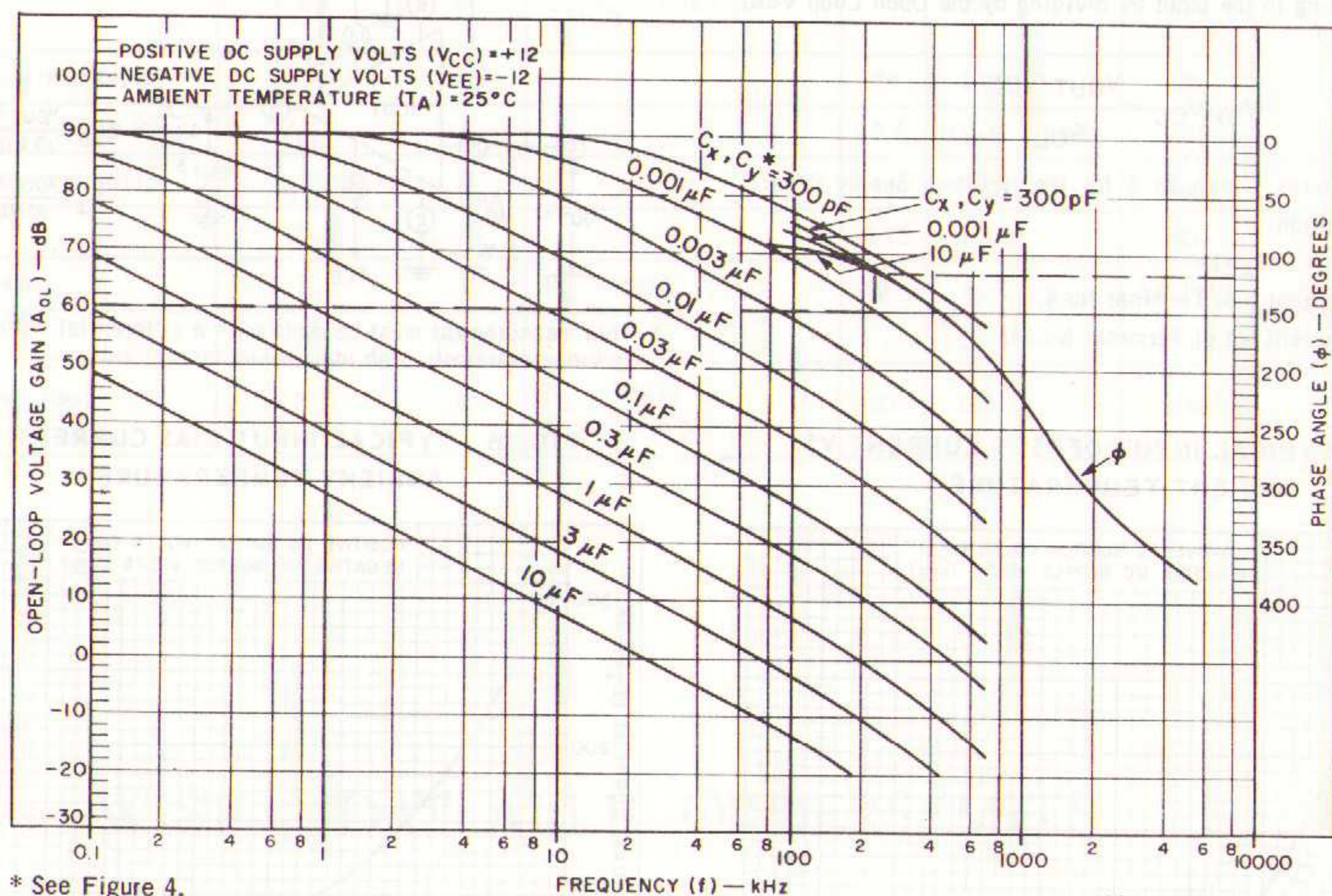


7. Calculate Output Current and Power Output

$$I_o = \frac{V_{o\text{ p-p}}}{500}$$

$$P_{out} = \frac{V_o^2(\text{rms})}{500}$$

FIG.4B - TYPICAL PHASE COMPENSATION CHARACTERISTICS ($V_{CC} = +12V$, $V_{EE} = -12V$)



* See Figure 4.

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A

minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network.

Figure 4C shows the phase compensating capacitors (C_x , C_y) returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V_{EE}) supply may result in more stable operation.

[illegible]

92CS-15291

POSITIVE DC SUPPLY VOLTS (V_{CC})
NEGATIVE DC SUPPLY VOLTS (V_{EE})
AMBIENT TEMPERATURE (T_A) = 25°C
FREQUENCY (f) = 1 kHz

PEAK-TO-PEAK OUTPUT CURRENT (I_O)P-P—mA

80
60
40
20

0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9

LOAD RESISTANCE R_L —K OHMS

$V_{CC}=+12V$
 $V_{EE}=-12V$

92CS-15292

POSITIVE DC SUPPLY VOLTS (V_{CC})
 NEGATIVE DC SUPPLY VOLTS (V_{EE})
 AMBIENT TEMPERATURE (T_A) = 25°C
 FREQUENCY (f) = 1 kHz

POWER TO LOAD (P_o) — mW

LOAD RESISTANCE R_L — K OHMS

$V_{CC} = +12\text{V}$
 $V_{EE} = -12\text{V}$

92CS-15293

The diagram shows a differential amplifier circuit using an ICUT (IC 741) op-amp. The circuit includes a 20V supply, a 1K resistor, a 1M resistor, a 51 resistor, a 100 microF capacitor, a 1KHz signal source, a DC voltmeter (RCA WV-38A or equivalent), and an oscilloscope (Tektronix Type 502A or equivalent). The output is measured at VOUT (DC) and VOUT (1 kHz).

92CS-15294

Procedure:

COMMON-MODE REJECTION RATIO:

1. Set $V_{BIAS} = 0$. Adjust V_E for $V_{OUT(DC)} = 0 \pm 0.1$ V.
2. Apply 1-kHz sinusoidal input signal and adjust for $V_S = 1.0$ V (RMS).
3. Measure and record the RMS value of V_{OUT} . An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:
 $ACM = V_{OUT}/V_S$
 $ACM \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$
5. Calculate Common-Mode Rejection Ratio:
 $CMR \text{ in dB} = A_{DIFF} \text{ in dB} - ACM \text{ in dB}$.

COMMON-MODE INPUT-VOLTAGE RANGE:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

FIG.5A - TYPICAL COMMON MODE REJECTION VS. AMBIENT TEMPERATURE

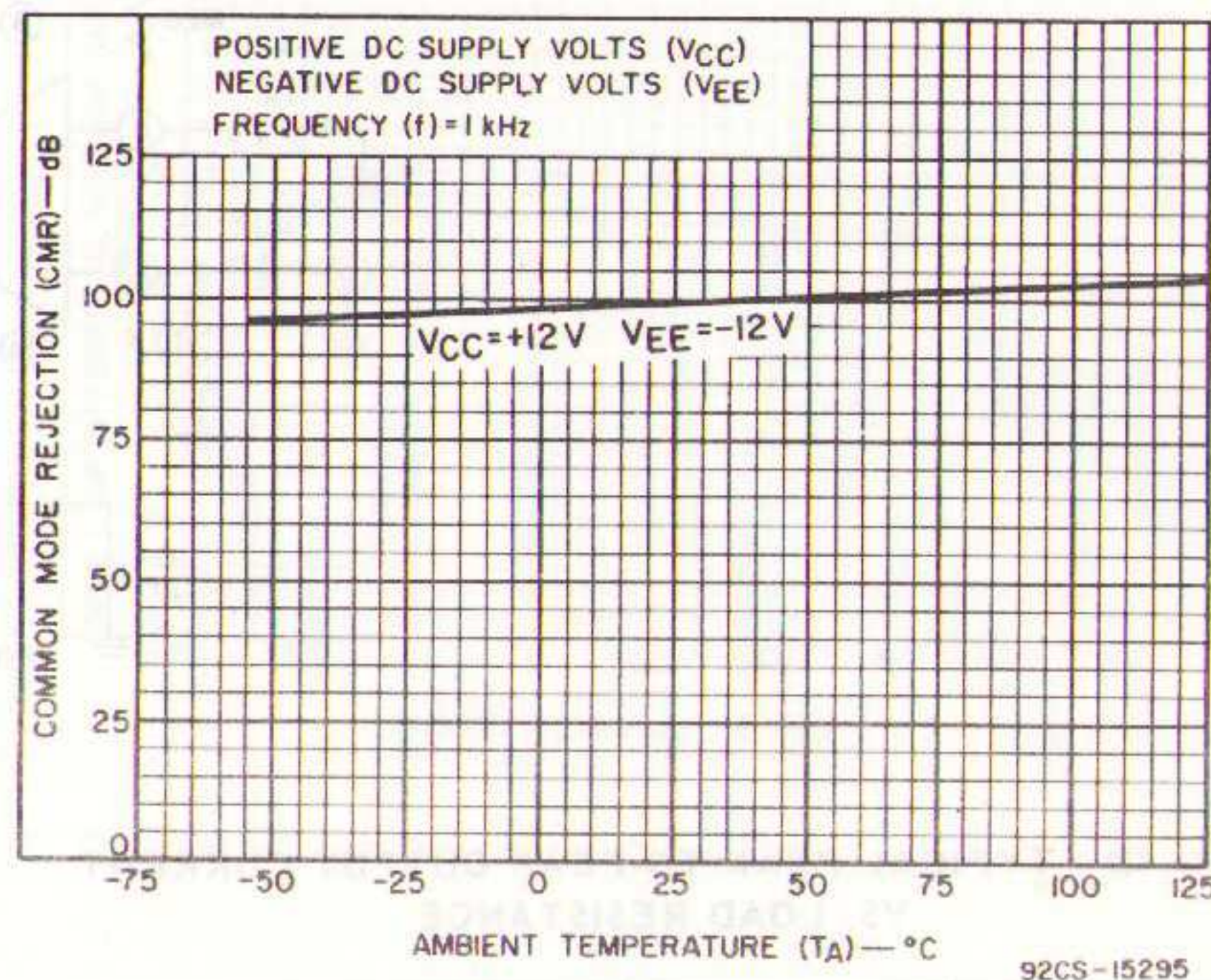
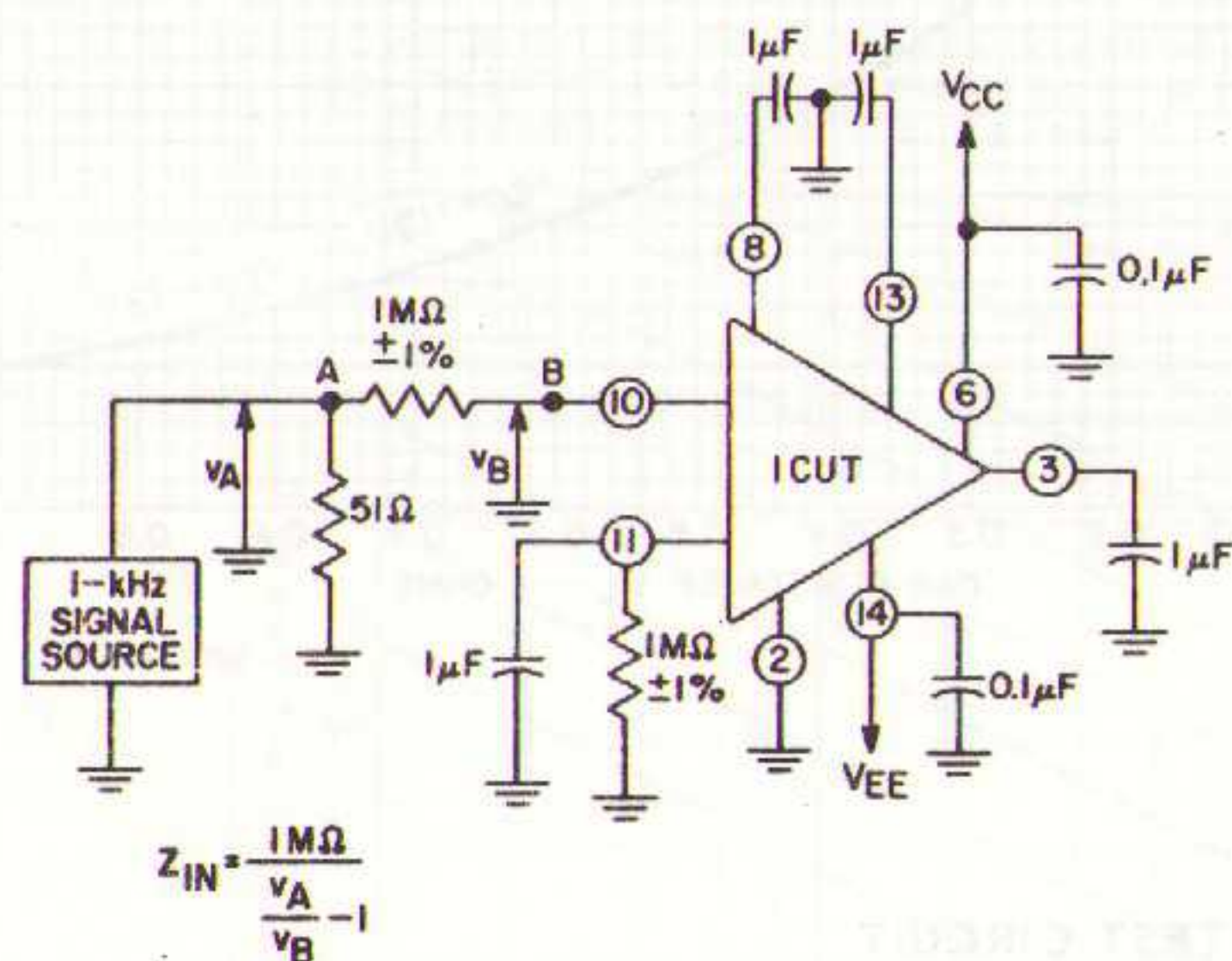
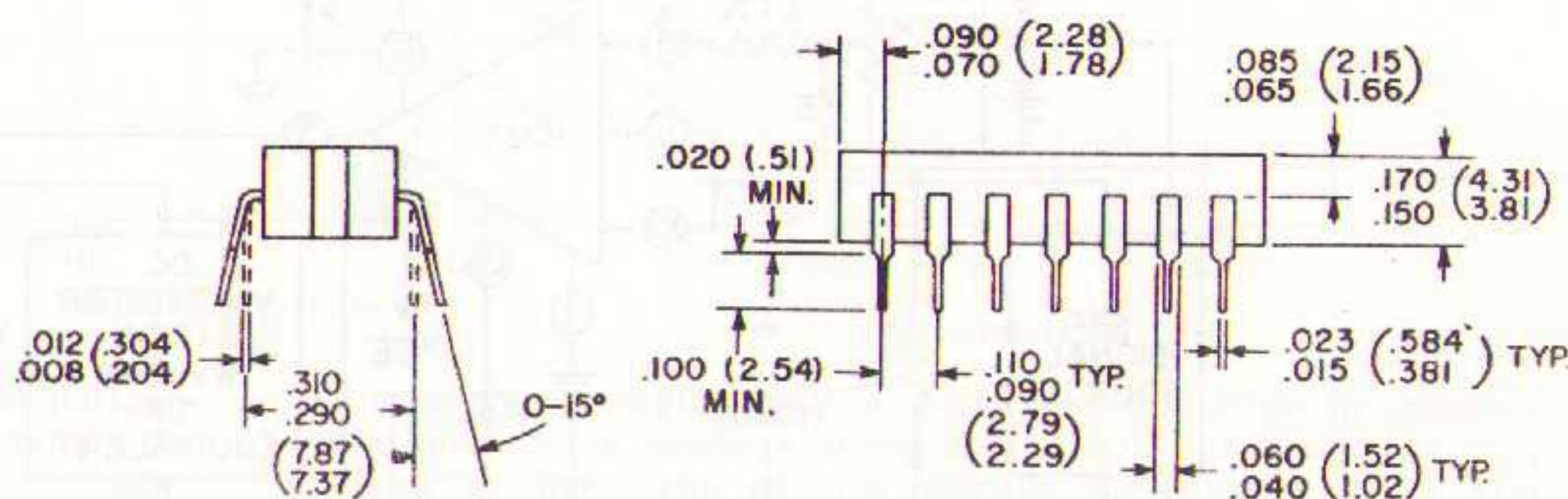
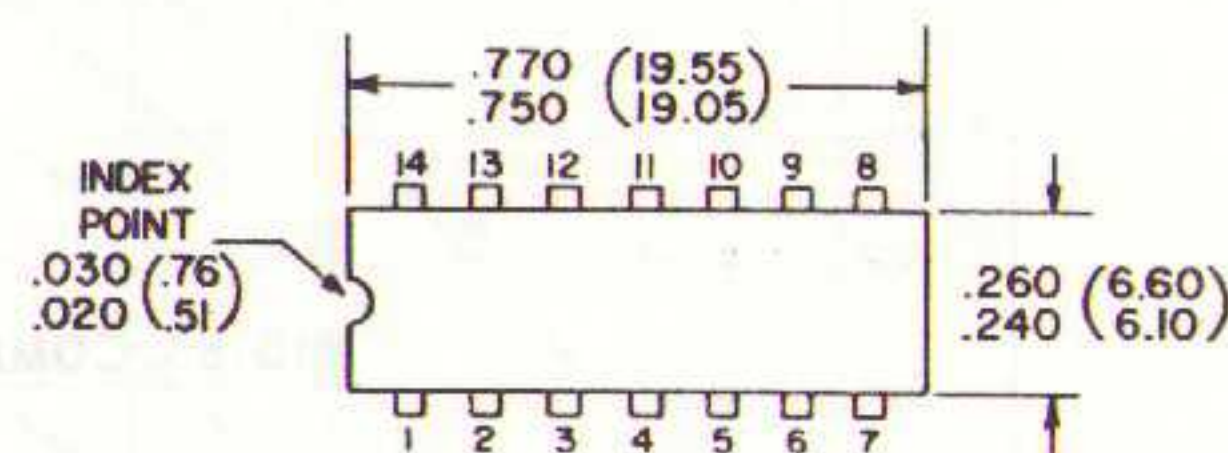


FIG.6 - SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

DIMENSIONAL OUTLINE
JEDEC TO-116

DIMENSIONS IN INCHES AND MILLIMETERS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

DIEVEN!

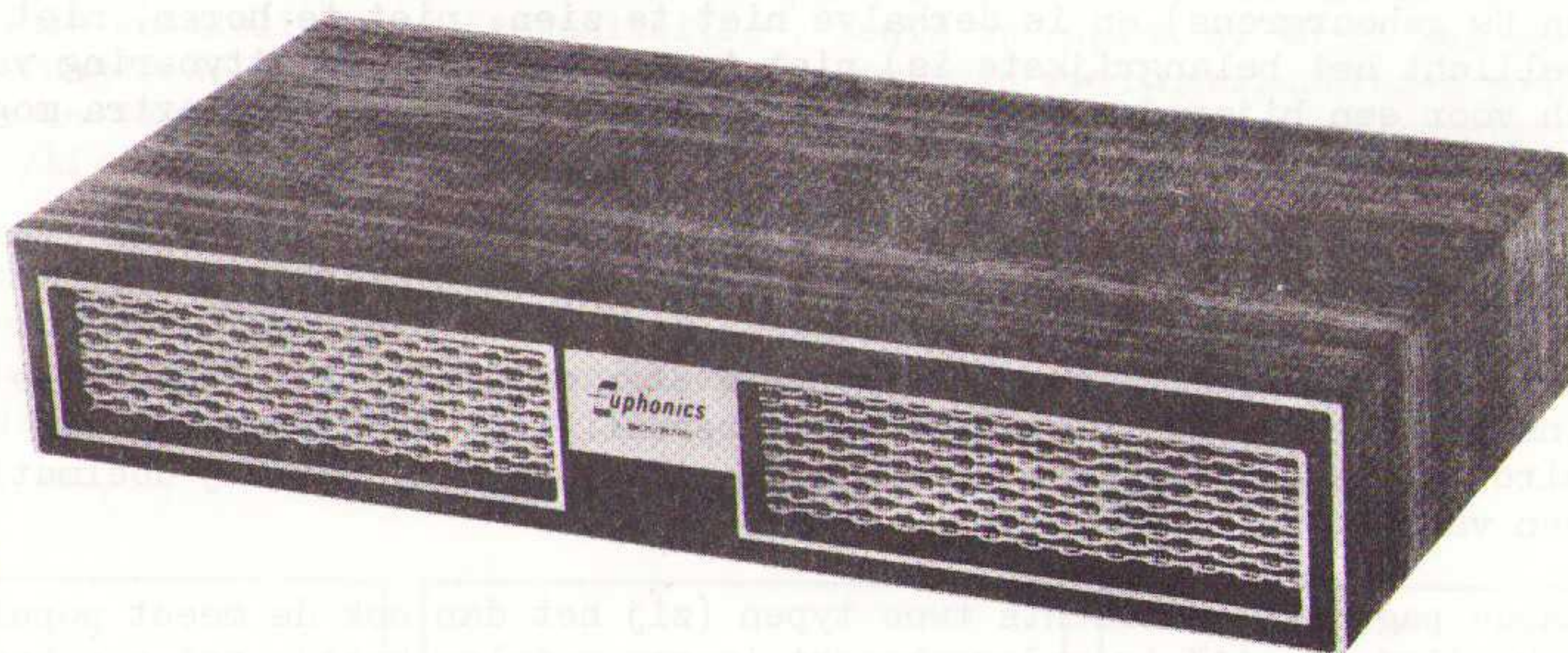
Dat kan vanochtend uw uitroep geweest zijn toen u bemerkte, dat u vannacht bezoek heeft gehad van inbrekers. Wellicht bent u goed tegen inbraak verzekerd, maar ontvangt u ook een schadevergoeding voor het vele extra werk en de narigheid die uit dit bezoek gaat voortvloeien of is dit voldoende voor de onvervangbare artikelen?? Dat natuurlijk niet, daarom is voorkomen beter dan genezen. Dat voorkomen kan met behulp van

ULTRASONISCHE INBRAAK- EN
BRANDBEVEILIGINGSAPPARATUUR

van



Sinds april '71 hebben wij de alleenvertegenwoordiging voor de Benelux van Bourns Security Systems Inc. USA op ons genomen en ons leveringsprogramma uitgebreid met onder andere de volgende beveiligingsapparatuur:



Type A4 X

A4x

Dit ultrasonische beveiligingsapparaat straalt een frequentie uit binnen een gebied van 7 meter; zodra hierin een beweging gesignaleerd wordt, schakelt de beveiliging in en kan de gehele verlichting in het pand of een stil alarm ingeschakeld worden. Het apparaat is ook voorzien van aansluitingen voor deur- en raamschakelaars, paniekschakelaars en temperatuurvoelers voor brandbeveiliging. Voor gebruik in één ruimte kunnen verschillende frequentiegebieden geleverd worden, waardoor onderlinge beïnvloeding voorkomen kan worden. De A4 X is tevens geschikt voor aansluiting op een 12 volt noodinstallatie.

..... prijs excl. 14% B.T.W. f 595,=

ACA150x

Dit apparaat heeft dezelfde technische eigenschappen als de A4 X, doch is niet geschikt voor een 12 volt noodinstallatie maar ondergebracht, tesamen met een bel van 25 cm Ø in een als luidsprekerbox uitziend walnoten kastje. Ook dit type kan worden voorzien van bovenstaande extra schakelaars. De ACA150 X is door zijn vormgeving bijzonder onopvallend en kan eenvoudig verplaatst worden.

..... prijs excl. 14% B.T.W. f 775,=

Voor bovenstaande en andere typen beveiligings-apparatuur zijn vele accessoires leverbaar, waaronder panieklampen, sirenes, bellen, temperatuurvoelers, afstandsschakelaars, enz. Nadere inlichtingen worden u op aanvraag gaarne verstrekt door uw beveiligings-installateur of:

van dam
ELEKTRONICA

Alleenvertegenwoordiger voor de Benelux landen:
N.V. Technische Handelmaatschappij Van Dam Elektronica
Afdeling: wetenschappelijke apparatuur. Postbus 3149,
Rotterdam-noord, Holland. Telefoon: (010)-245516-240812-
243497. Postgirorekening: 295550. Bankier: Amro-bank.

Bourns' ultrasonische inbraak- en brandbeveiligingen.

Inleiding.

Inbraken zijn tegenwoordig dagelijks in het nieuws: leest U Uw dagblad maar eens; er staat er ongetwijfeld wel weer een in! Dat is dan nog plaatselijk. Laten we dus maar niet denken aan wat er landelijk die nacht aan inbraken heeft plaatsgehad en dié inbraken, welke de kranten niet vermelden! Vandaag is het misschien Uw buurman; morgen kunt U echter het slachtoffer zijn van een brutale inbraak. Indien U zich hiertegen wilt beschermen, kunt U verscheidene soorten inbraakbeveiligingen aanschaffen, waarvan de prijs evenveel varieert als de doelmatigheid.

Deze twee factoren zijn ook van doorslaggevende betekenis geweest toen wij de inbraak- en brandbeveiligings apparatuur van Bourns Security Systems Inc. USA aan ons voorraadprogramma toevoegden. Deze beveiligings-apparatuur werkt op een ultrasonische frequentie (boven Uw gehoorrens) en is derhalve niet te zien, niet te horen, niet te ruiken, en (wat wellicht het belangrijkste is) niet te beïnvloeden. De uitvoering van Bourns leent zich voor een bijzonder groot toepassingsgebied door de vele extra mogelijkheden, welke op deze apparatuur aanwezig is.

Technische aspecten.

Een goede inbraakbeveiliging mag niet te saboteren zijn; dit is een kwestie van aanleg der installatie of, bij wijze van extra beveiliging, de toevoeging van een kabelcontrolecircuit. Tevens mag zo'n beveiliging niet opvallen. Dat hij doelmatig moet zijn is een vanzelf sprekende zaak.

Op voorgaande pagina zijn slechts twee typen (zij het dan ook de meest populaire typen) aangekondigd. De A4X is ondergebracht in een metalen kastje met een houtkleurige verflaag en een bijzonder fraai tonend front. Dit type kan in een modern interieur of zakenpand worden geplaatst, zonder hier op te vallen. Het vormt echter een gevoelig beveiligingsapparaat, dat in staat is Uw eigendommen in de ruimte, waar het geïnstalleerd is, optimaal te beveiligen. Hierbij kan de A4X worden gevoed vanuit het 220 V. lichtnet of een 12 volt noodinstallatie. Zo'n noodinstallatie kan bij het uitvallen of uitschakelen van de 220 V. bron uw beveiligingssysteem in tact houden. Zodra binnen de bewaakte ruimte op minder dan ca. 7 meter van het apparaat een beweging plaatsvindt, schakelt de beveiliging zijn 1ste contact: hiermee wordt een 220 V. - 660 Watt uitgang geschakeld, van waaruit de alarmering (relais voor het inschakelen van de gehele verlichting in het pand of een panieklamp of een schijnwerper) kan worden gevoed.

Ongeveer 10-20 seconden na het sluiten van het eerste contact, sluit zich een 2de contact, dat op de 220 V. maximaal 100 watt en op de 12 volt (noodinstallatie) maximaal 12 watt. Dit vermogen kan worden gebruikt voor het voeden van een sirene, bel, toeter, zwaailicht, automatisch sluitende deuren, valluiken, "inbrekers knock-out apparaat", enz., enz. Wat er daarna gebeurt, hangt van de doelmatigheid van Uw signaleringen af. Hoe U zelf wel bij Uw eigendommen kunt en de juiste werking van het alarmeringssysteem wordt U verteld in de bij het apparaat geleverde gebruiksaanwijzing

De ACA 150X is uitgerust met een 220 V. uitvoering van de A4X (de A5X) en ziet eruit als een luidsprekerkastje van notenhout. Ook deze uitvoering behoeft niet op te vallen in Uw interieur. Deze uitvoering is niet geschikt voor 12 V. en werkt verder als de A4X. Het tweede contact schakelt echter geen externe alarmeringsbronnen maar de ingebouwde krachtige 25 cm. bel, die voor de nodige akoestische begeleiding van de door het eerste contact geschakelde alarmering zorgt.

Op deze beide apparaten kan ook een serieketen van magnetische deur- en raamcontacten, thermocontacten (voor gebruik als brandalarm!), paniekdruktoetsen, vloercontacten, enz. worden aangebracht. Een onderbreking in deze keten doet het alarm inschakelen en dient als extra beveiliging voor de ruimten, waarop dit apparaat geen ultrasonische invloed heeft. Wilt U nadere inlichtingen? Schrijft U dan vandaag nog een briefje! Morgen kan er al ingebroken worden

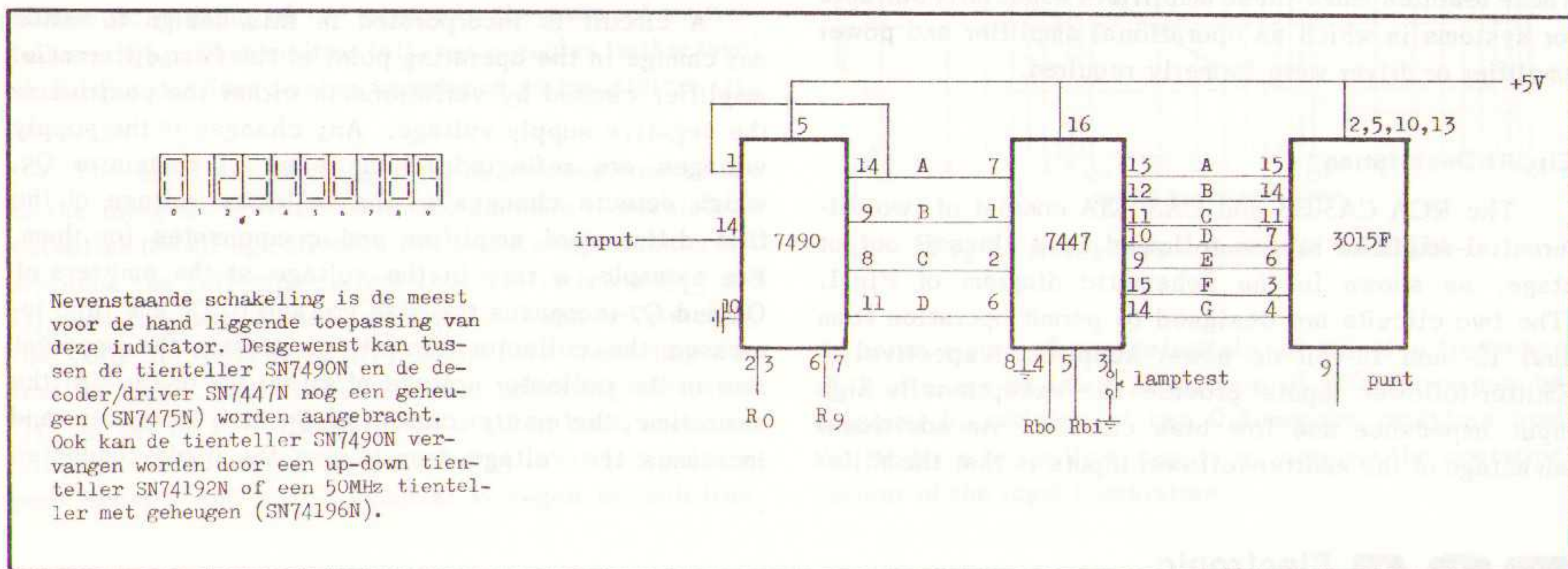
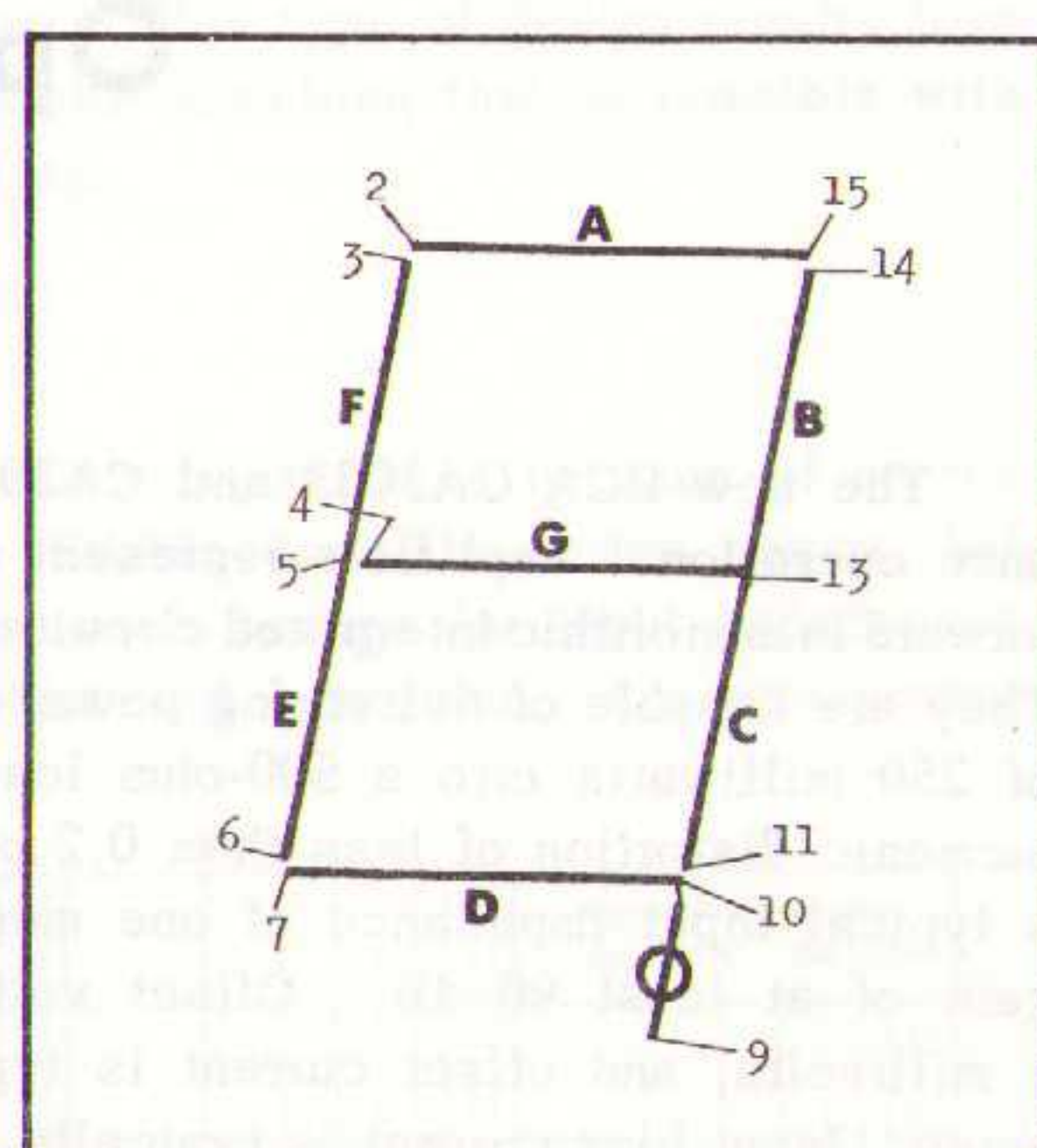
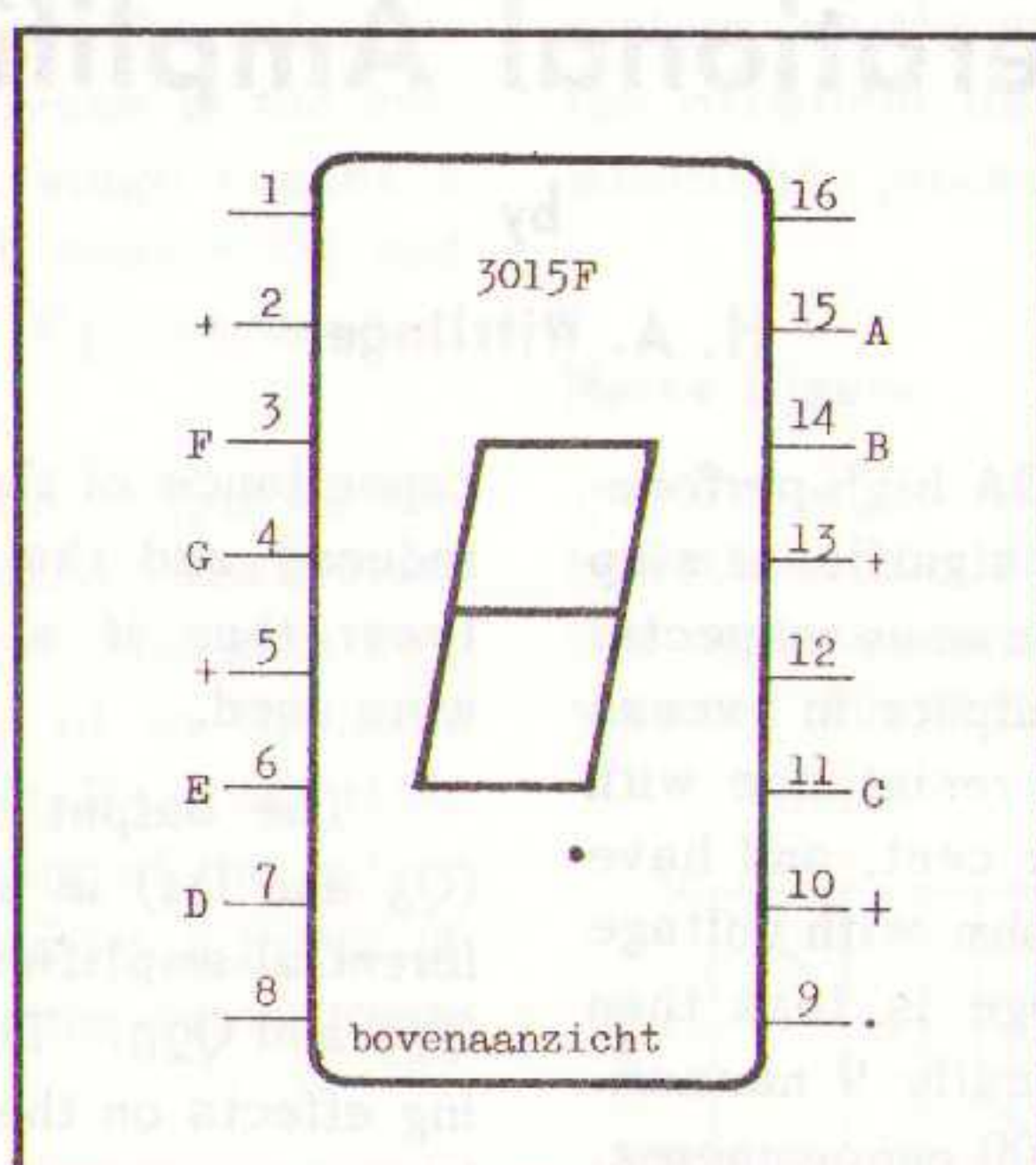
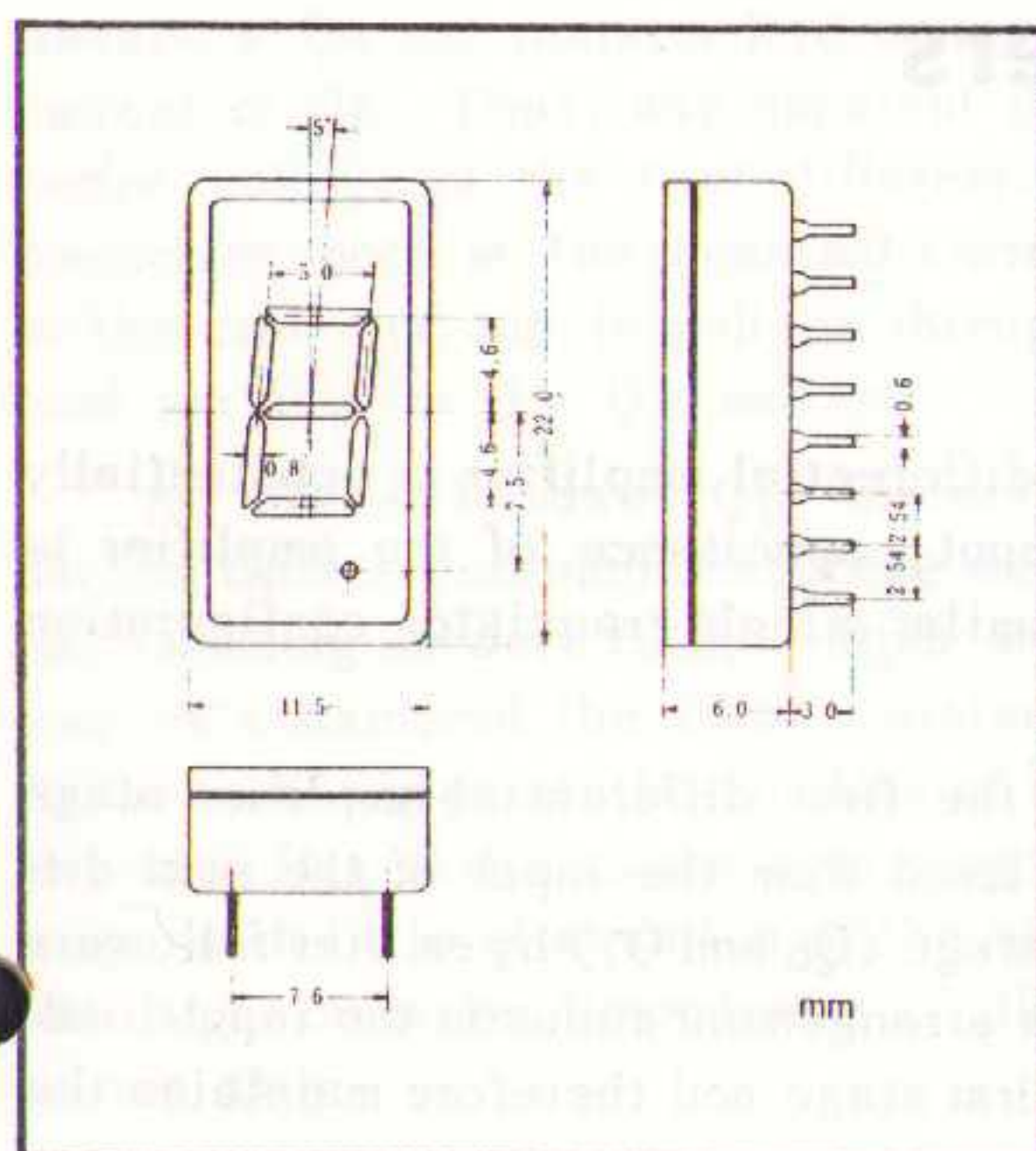
Digitale multimeter voor zelfbouw.

Op pagina 26 t/m 32 hebben wij de volledige technische gegevens opgenomen van de RCA CA 3047. Deze geïntegreerde schakeling is de commerciële uitvoering van de CA 3033, waarover op de navolgende pagina's 36 t/m 43 meer is opgenomen.

De CA 3047 is alleen al om zijn eigenschappen interessant: een open-loop-gain van 90dB typ. en een ingangsimpedantie van 1,5MΩ opent voor een operationele versterker een interessant toepassingsgebied. Als dan ook nog op pagina 41-43 een interessante toepassing als goedkope digitale multimeter is opgenomen, dan kunnen wij ons levendig indenken, dat vele lezers vol interesse deze pagina willen omslaan.

Doet U dit gerust, nadat wij U er eerst nog op attenderen, dat onderstaande schakeling als "totaalteller", zoals op pagina 41 wordt genoemd, kan fungeren. Hierdoor heeft U nog slechts twee voedingsspanningen nodig: voor de tellers en indicators: +5 volt en voor de AD converter/reseteenheid/tijdbasis + en - 12 volt.

Technische details voor de voor de verdere afbouw van deze digitale multimeter in aanmerking komende digitale geïntegreerde schakelingen werden opgenomen in onze Technische Documentatie 1970 (nog beperkt compleet leverbaar voor f 10,40 per vooruitbetaling op postgiro 29 55 50 onder vermelding van "voor TD 1970".)



RCA integrated circuits application note



ICAN-5641

Application of RCA CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers

by

H. A. Wittlinger

The new RCA CA3033 and CA3033A high-performance operational amplifiers represent a significant step forward in monolithic integrated circuits in many respects. They are capable of delivering power outputs in excess of 250 milliwatts into a 500-ohm load resistance with harmonic distortion of less than 0.2 per cent, and have a typical input impedance of one megohm with voltage gain of at least 90 dB. Offset voltage is less than 5 millivolts, and offset current is typically 9 nanoamperes. Input bias current is typically 100 nanoamperes. These features make these amplifiers especially suitable for systems in which an operational amplifier and power amplifier or driver were formerly required.

Circuit Description

The RCA CA3033 and CA3033A consist of two differential-amplifier stages followed by a class B output stage, as shown in the schematic diagram of Fig.1. (The two circuits are designed to permit operation from dual 12- and 18-volt dc power supplies, respectively.) Emitter-follower inputs provide the exceptionally high input impedance and low bias current. An additional advantage of the emitter-follower inputs is that the Miller

capacitance of the differential amplifier is substantially reduced and the input capacitance of the amplifier is lower than if a similar single-transistor configuration were used.

The output of the first differential-amplifier stage (Q3 and Q4) is buffered from the input of the next differential-amplifier stage (Q6 and Q7) by emitter followers Q19 and Q20. This arrangement reduces the input-loading effects on the first stage and therefore maintains the first-stage gain.

A circuit is incorporated in this design to sense any change in the operating point of the first differential amplifier caused by variations in either the positive or the negative supply voltage. Any changes in the supply voltages are reflected to the base of transistor Q5, which detects changes in the collector voltage of the first differential amplifier and compensates for them. For example, a rise in the voltage at the emitters of Q6 and Q7 increases the bias voltage to Q5 and thus increases the collector current, countering the apparent rise in the collector voltage of either Q3 or Q4. At the same time, the emitter current of Q5 also increases, and increases the voltage drop across the diode-connected

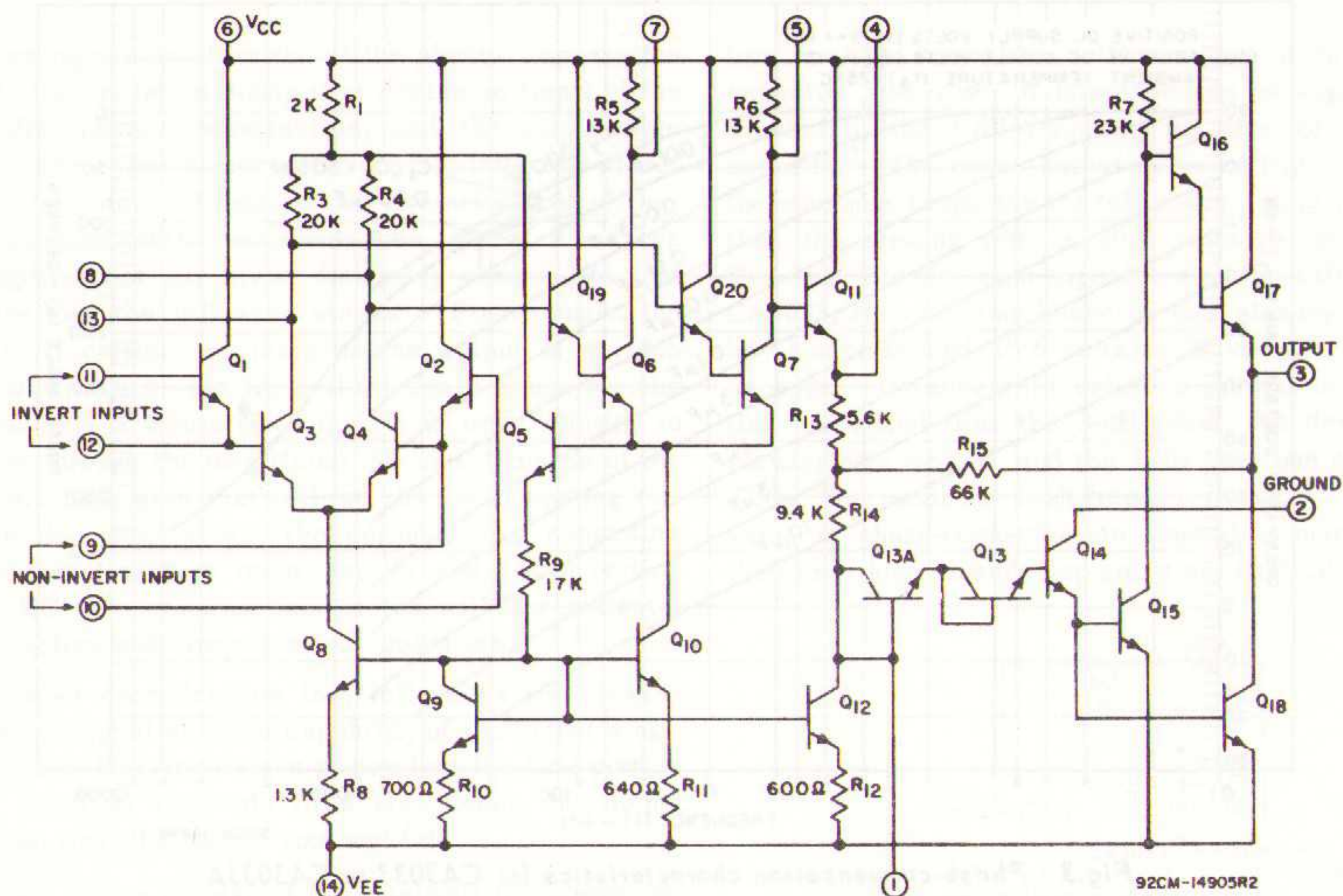


Fig.1 - Schematic diagram of a CA3033 or CA3033A operational amplifier.

transistor Q9 and resistor R10 to increase the collector current of Q8. Thus, any apparent increase in the collector voltage of the first differential stage causes a correction both at the constant-current source Q8 and at the collector supply voltage through R1, the common load resistor for Q3, Q4, and Q5.

An emitter-follower Q11 buffers the output of the second differential-amplifier stage and drives the divider and summing network to the output stage. Resistor R13 may be considered the input resistance of an amplifier to the summing point, the junction of R13, R14, and R15. Resistor R14 shifts to the operating point of the output stage with little attenuation of the signal as a result of the high collector impedance of the constant-current source Q12.

Diode-connected transistors Q13A and Q13 provide further dc shifting of the signal to the base of emitter-follower Q14. This emitter-follower provides further level shifting and a low driving impedance to transistors Q15 and Q18.

The excellent matching of the base-to-emitter voltage of the integrated-circuit transistors makes it possible to establish the idling current of the output stage accurately. Because the collector-current characteristics of Q15 and Q18 as a function of base-to-emitter voltage are matched, the collector current in Q15 determines the idling current in Q18. For example, if the operating current of Q15 is set at 1 milliamperes for a given base-to-emitter voltage, the operating current of Q18 is also 1 milliamperes because the base-to-emitter voltages of both transistors are the same.

This type of design results from the excellent transistor matching that is possible with monolithic processing.

Noise Figure

Fig.2 shows noise figure as a function of source resistance for the CA3033A. The curve shows that the optimum noise match occurs for input impedances between 100,000 ohms and 1 megohm. An improvement

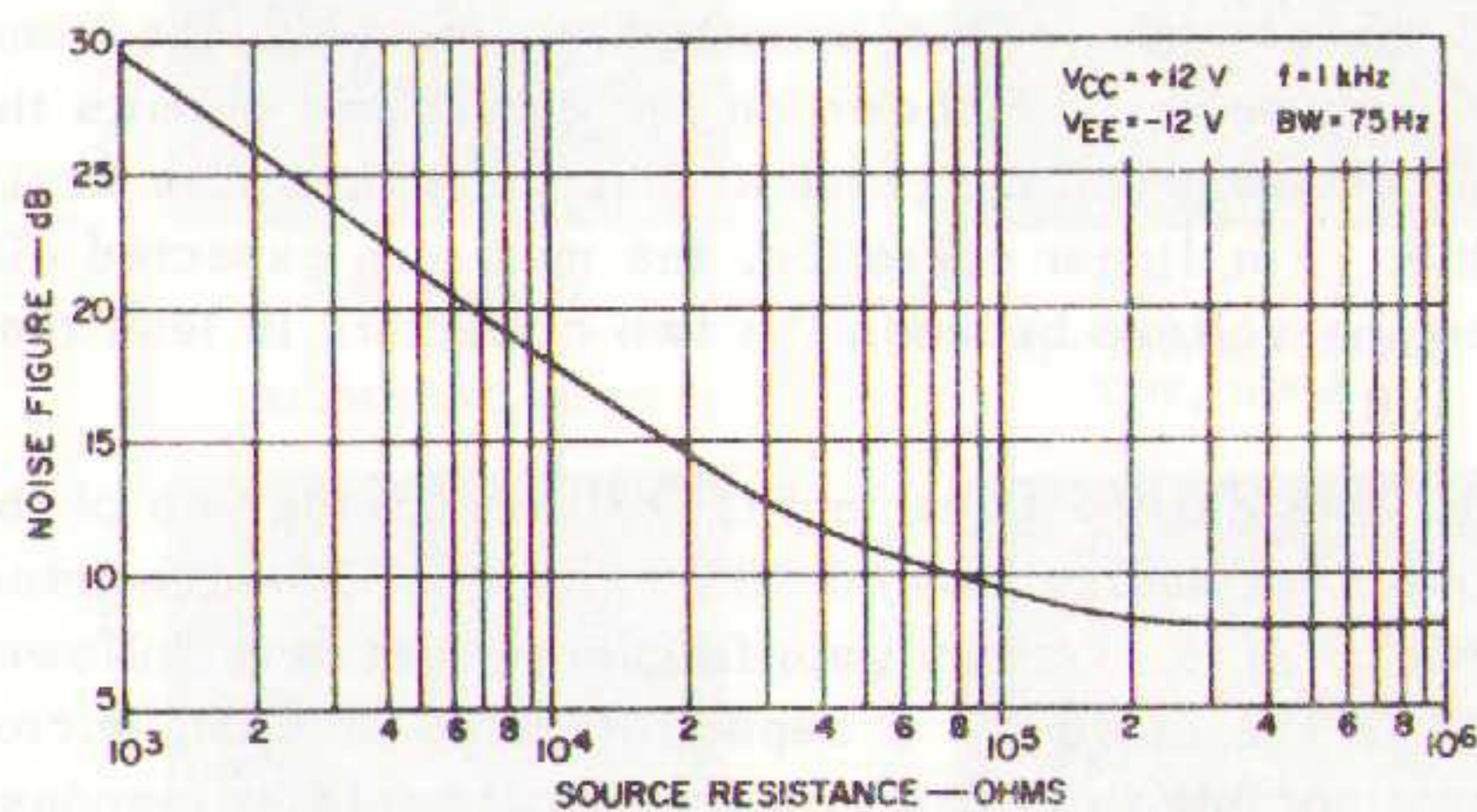


Fig.2 - Noise-figure curve for CA3033A.

in noise figure of approximately 14 dB at a frequency of 1 kHz and an input impedance of 1000 ohms may be obtained by addition of two 0.3-megohm resistors from the emitters to the VEE supply to increase the operating current of the input transistors.

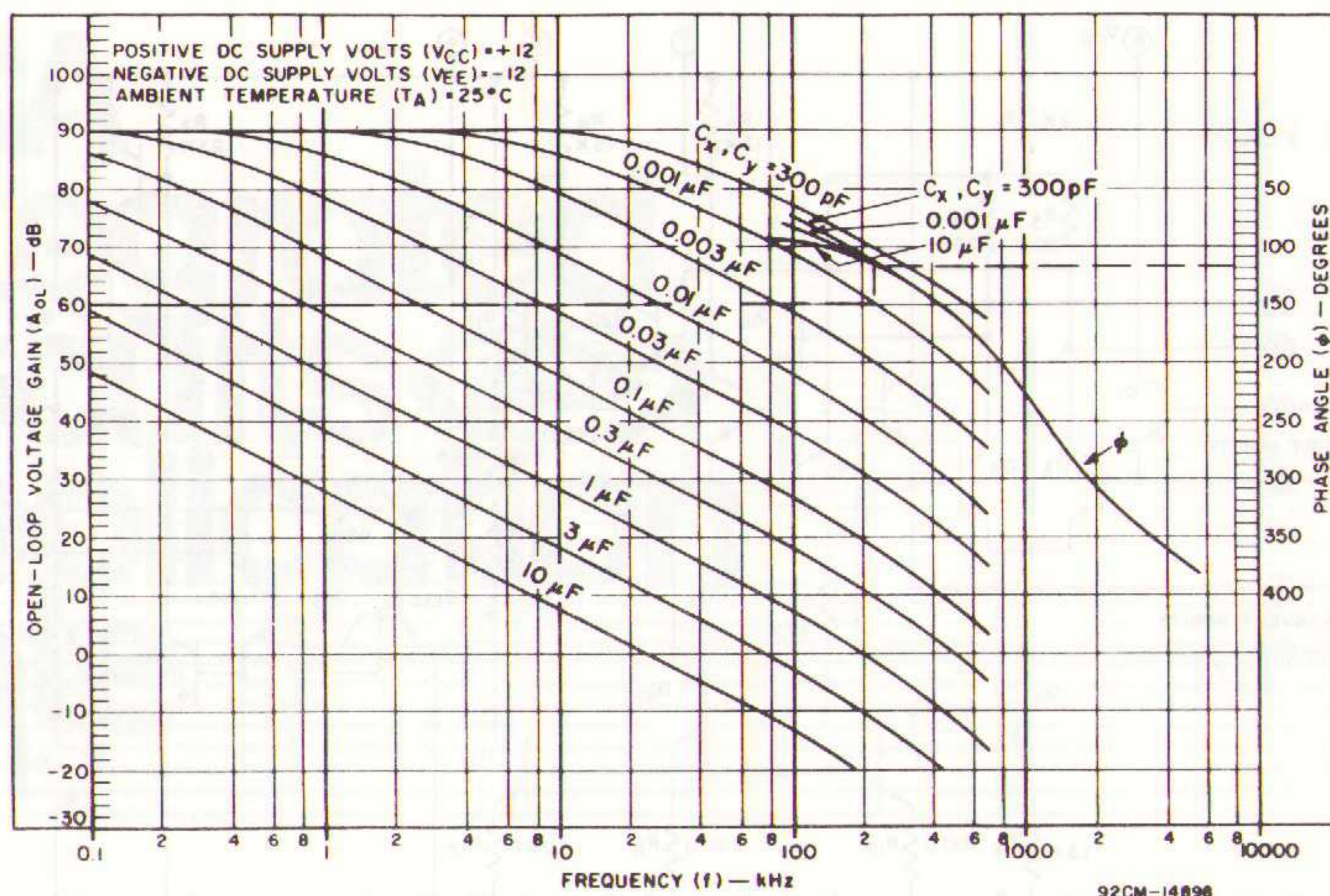


Fig. 3 - Phase-compensation characteristics for CA3033 or CA3033A.

Compensation

Basic phase compensation of the CA3033 and CA3033A amplifiers is quite simple. Fig. 3 shows typical phase-compensation characteristics for the CA3033; data for the CA3033A are similar. The two compensating capacitors C_x and C_y are connected from the collectors of the first differential amplifier (terminals 8 and 13) to ground. When capacitance values greater than 0.1 microfarad are used, however, a lower-voltage capacitor that has a value equal to half that given on the curves may be connected between terminals 8 and 13, and a 0.001-microfarad capacitor connected from either terminal 8 or 13 to ground. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of lower-voltage ceramic disc capacitors now available. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

The dashed lines in Fig. 3 illustrate the use of the curves for design of a 60-dB amplifier. First, the intersection of the various gain-frequency curves is followed out to the curve for a capacitor value of 0.001 microfarad. At this point, the expected 3-dB amplifier response is approximately 230 kHz and the phase angle ϕ is 118 degrees; the phase margin ($180^\circ - \phi$) is thus 62 degrees. For a capacitance value of 300 picofarads, the expected 3-dB response is 580 kHz, but the phase angle is 175 degrees; the resulting phase margin of only 5 degrees is a most undesirable situation. In the other direction, the use of 0.003-microfarad compensating capacitors provides a 3-dB response of 90 kHz and a phase angle of

approximately 90 degrees, with a phase margin of 90 degrees.

Slewing Rate

One of the most important considerations in using a high-power operational amplifier such as the CA3033 or CA3033A is the maximum full power output swing in terms of frequency that can be expected from the unit. This characteristic is important both in low-frequency applications and in pulse applications in which the rise times of a given design must be known. Fig. 4 shows the maximum rate of change, or slewing rate, of a sine wave in volts per microsecond for various peak-to-peak output voltages.¹ For example, a 30-volt peak-to-peak sine wave at a frequency of 10 kHz has a maximum rate of change of 1 volt per microsecond. Besides being able to swing the value of 30 volts peak to peak at dc, therefore, an amplifier must also be able to swing this amplitude at a minimum rate of 1 volt per microsecond.

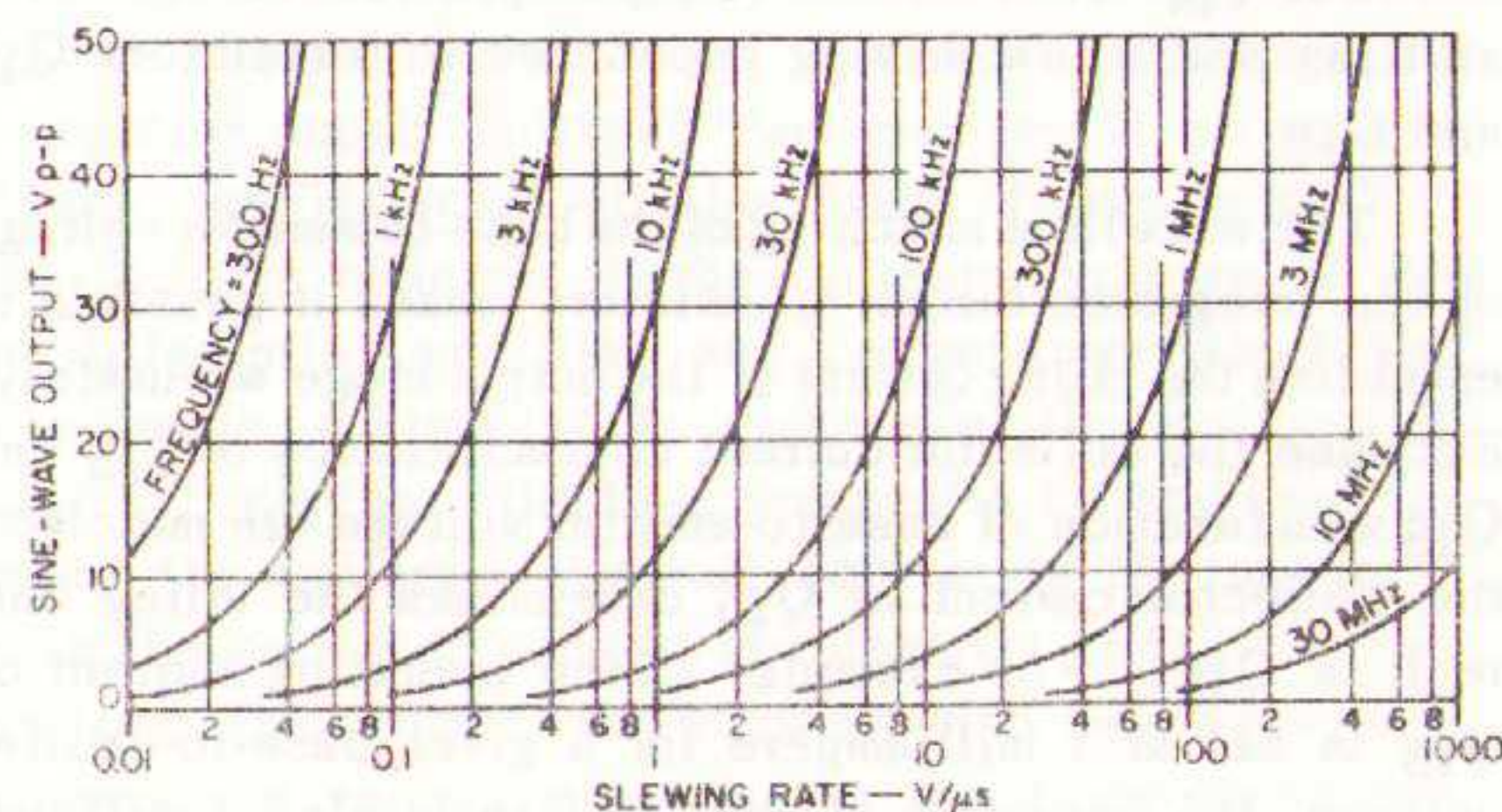


Fig. 4 - Slewing-rate curve.

Slewing rate is a function of the phase-compensation circuit, the operational-amplifier design in terms of the gain after phase compensation, and the output-stage design. The phase-compensation circuit is usually placed around the input stages of an operational amplifier. This approach offers two advantages. First, it reduces the amplitude of any higher-frequency components that may overload the following stages. (For example, the residual rf carrier remaining on the output of a video detector with a single RC roll-off could cause serious overload and a distorted output if it were allowed to continue through the amplifier.) Second, because of the relatively high gain that follows the compensating circuit in the input stage, the compensating capacitors charge and discharge on a smaller and faster portion of the RC time constant associated with the collector load resistors and compensation capacitors.

Another consideration that influences the slewing rate is the signal-handling capability of the output stage. It is evident that, regardless of how fast the first portion of an amplifier responds to a step input, the output stage can limit the rate of rise and fall.

Fig.5 shows a curve of the maximum full-power-output frequency of the CA3033 and CA3033A as a function of the phase-compensation capacitance. This curve may be used with the curve of Fig.4 to determine the amplifier slewing rate. In the case of the 60-dB amplifier shown in Fig.6, for example, two 0.002-microfarad capacitors are used for phase compensation. The curves of Fig.3 indicate that the 3-dB bandwidth is 120 kHz.

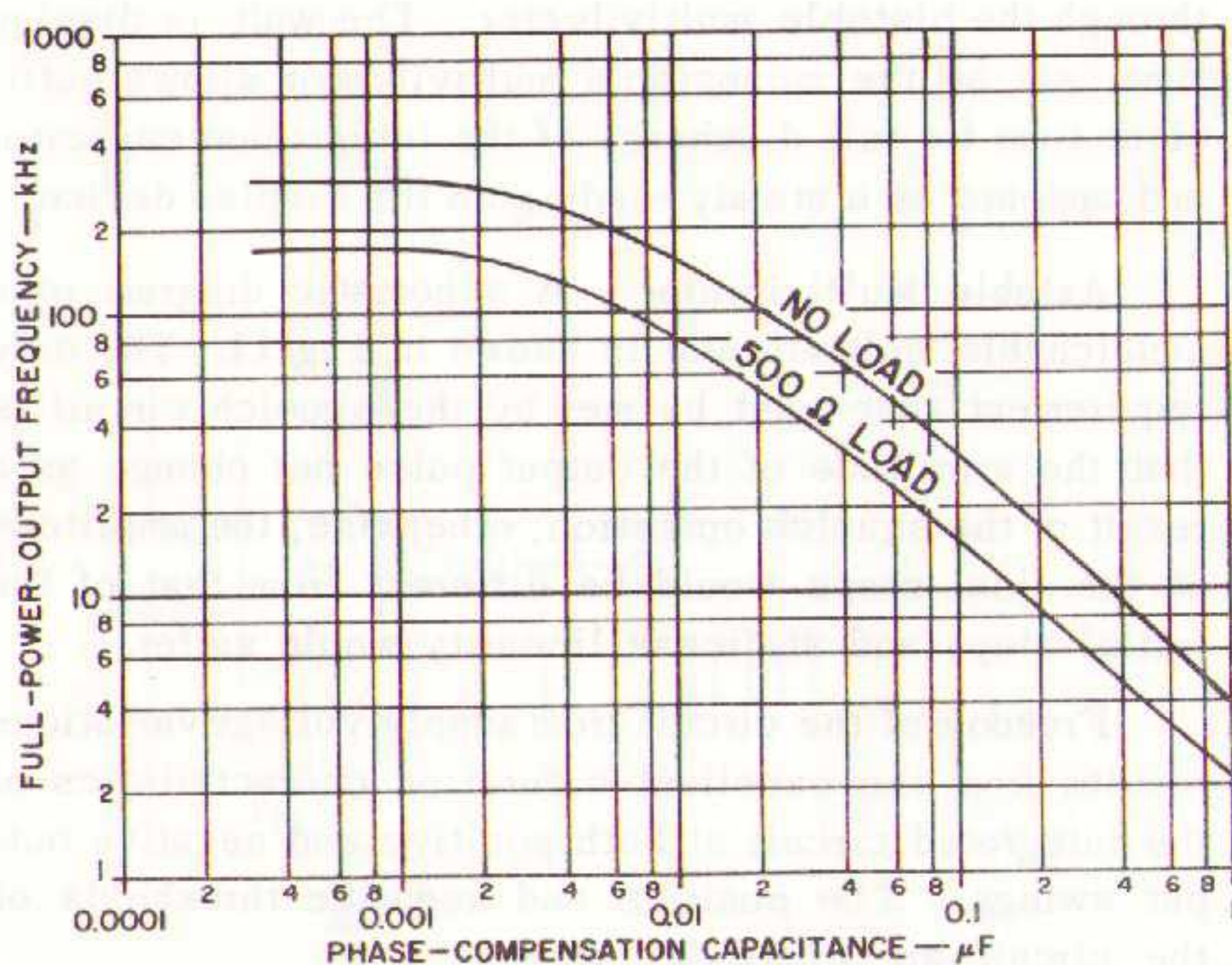
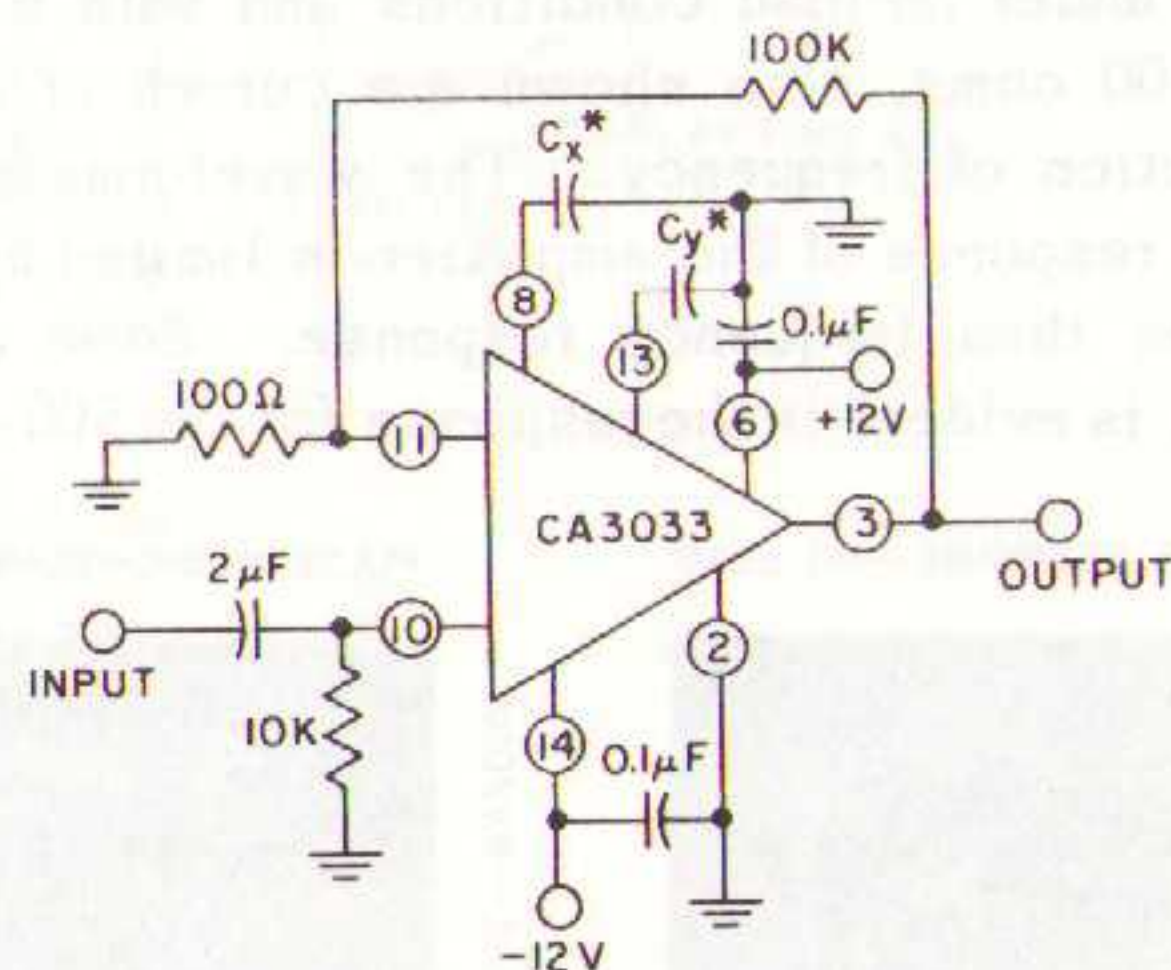


Fig.5 - Frequency for full power output as a function of phase-compensating capacitance.

Fig.5 shows that full output swing with no load may be expected up to a frequency of 280 kHz. Therefore, the design is capable of full power output up to the 3-dB point.

A similar approach may be used for a pulse amplifier. Two 0.01-microfarad phase-compensating capaci-

tors are used to yield a 3-dB response of 30 kHz. The expected rise time in microseconds is equal to 0.35 divided by the 3-dB frequency in MHz, or 11.7 microseconds.² The power-output curve of Fig.5 shows that the maximum frequency for full power output is 155 kHz; thus the slewing rate is 10.6 volts per microsecond. For the 20-volt input-signal swing specified for the CA3033, the rise time based on this slewing rate would be (1 microsecond/10.6 volts) x 20 volts, or 1.9 microseconds. Because this value is greater than the rise time estimated from the 3-dB point, the design is not slewing-rate limited, and the 3-dB rise time will be met. Thus, for maximum high-frequency output, the lowest value of phase-compensation capacitors must be used; therefore, high closed-loop gains are implicit.



*SEE TEXT FOR VALUES

Fig.6 - 60-dB test amplifier for CA3033.

Waveforms for the 60-dB amplifier are shown in Fig.7.

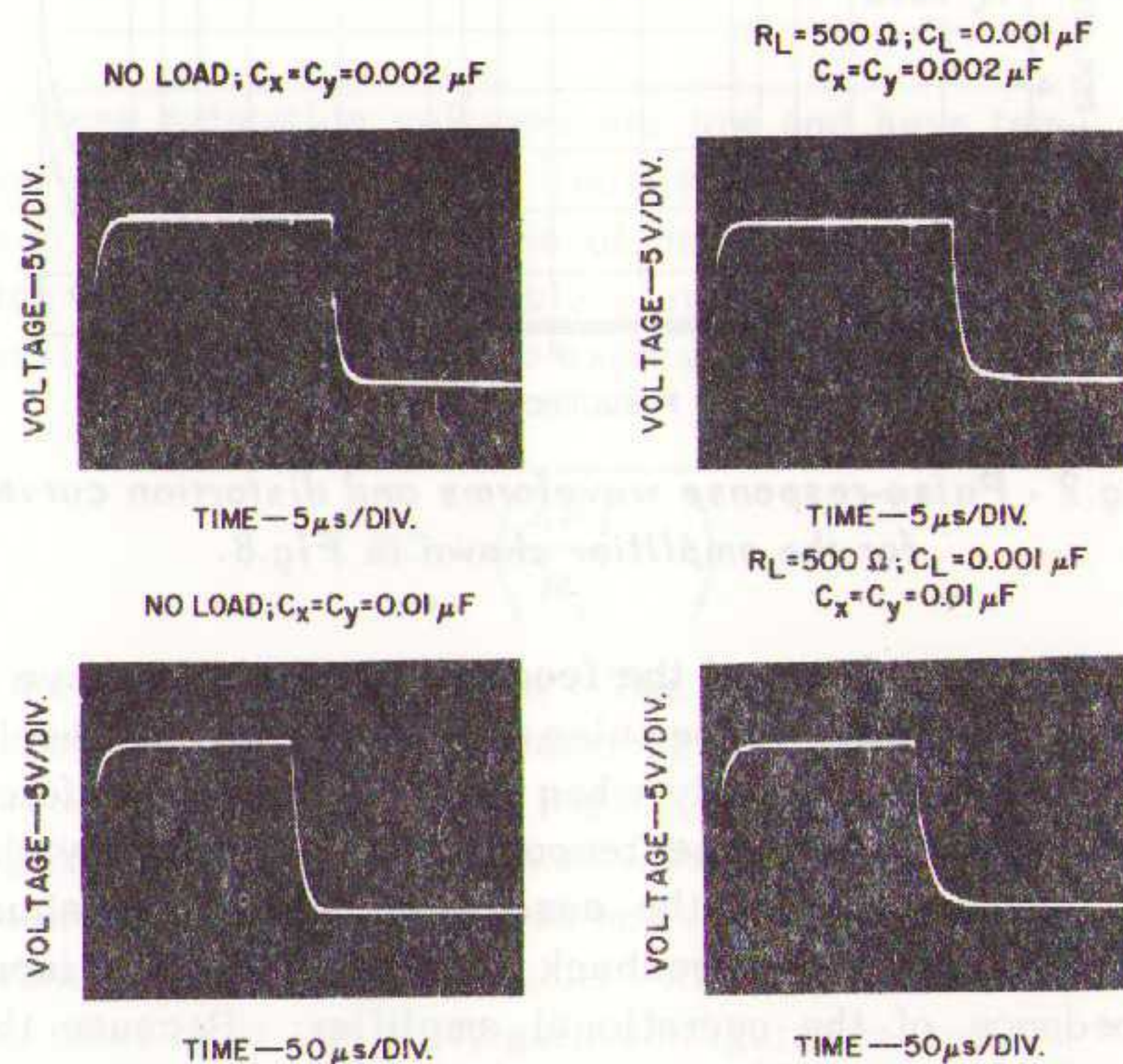


Fig.7 - Waveforms for the 60-dB amplifier shown in Fig.6.

Applications

Fig.8 illustrates the use of the CA3033A in a 20-dB, 255-milliwatt power amplifier operating from a single

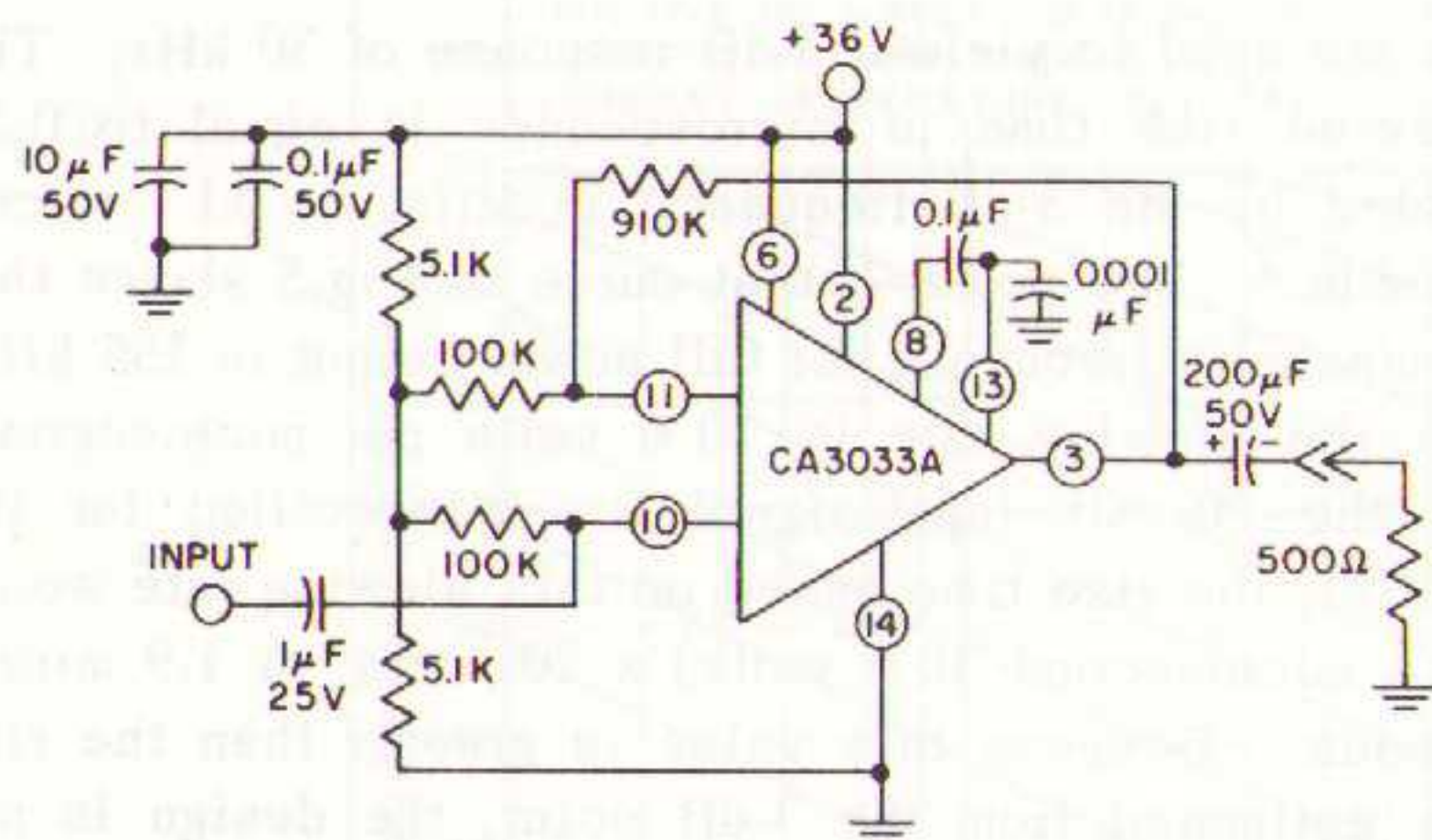


Fig. 8 - 20-dB, 255-milliwatt power amplifier using a CA3033A operating from a 36-volt supply.

36-volt supply. Fig. 9 shows the pulse response of this amplifier under no-load conditions and with a resistive load of 500 ohms; also shown are curves of distortion as a function of frequency. The waveforms show that the pulse response of the amplifier is limited by slewing rate rather than frequency response. Some crossover distortion is evident in the response for the 500-ohm load.

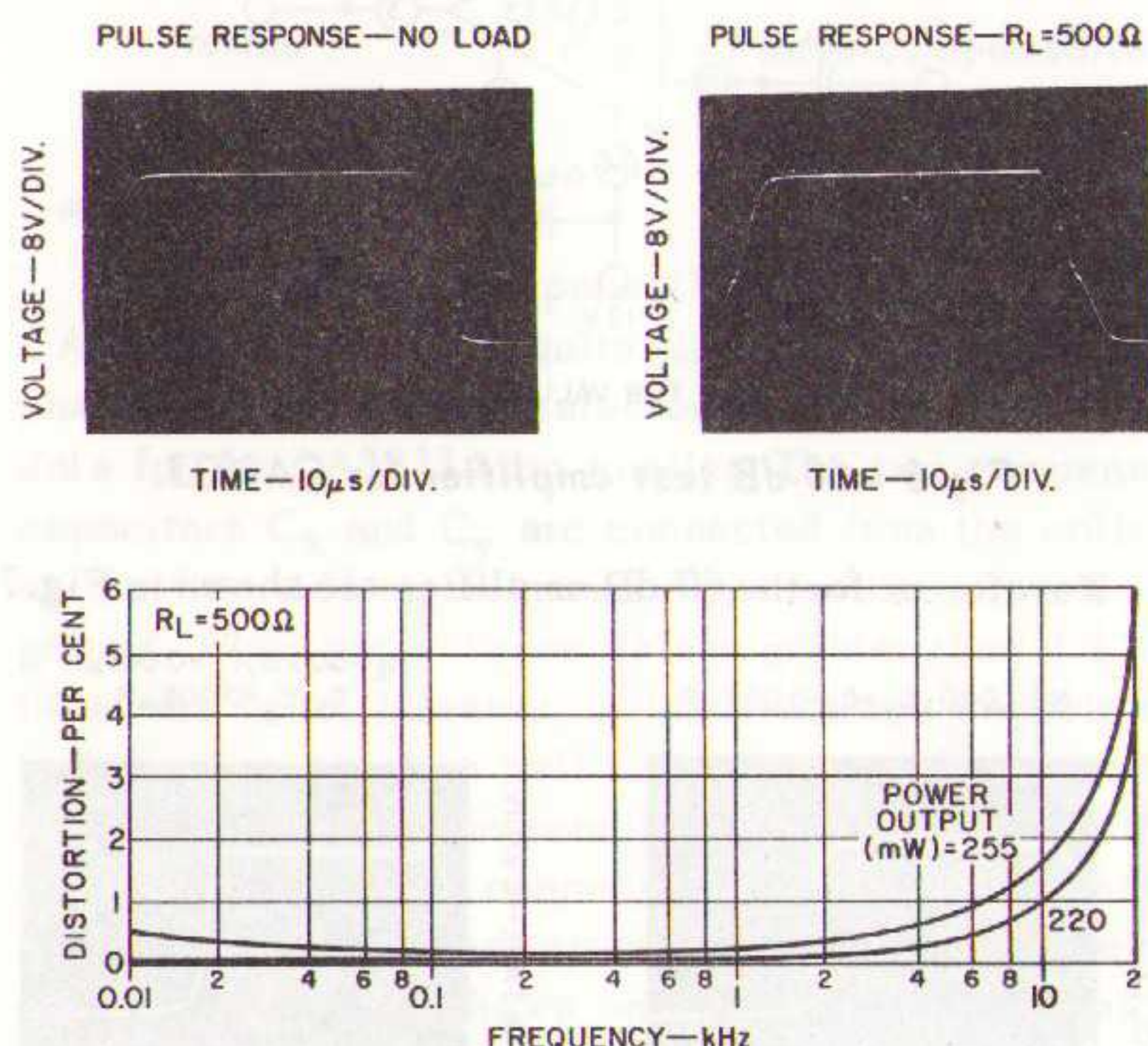


Fig. 9 - Pulse-response waveforms and distortion curves for the amplifier shown in Fig. 8.

The impedance of the feedback network can have a significant effect on the pulse response of a given amplifier design, particularly when higher-frequency performance is required. The response is influenced by the stray capacitance of the associated wiring, the shunt capacitance of the feedback resistors, and the input impedance of the operational amplifier. Because the CA3033 and CA3033A have higher input impedance as a result of the emitter-follower inputs, the input capacitive loading is reduced considerably and higher-impedance feedback networks can be used.

A simple system was fabricated to demonstrate the ease with which the CA3033 and CA3033A operational amplifiers may be applied. The basis of the system was

the rudiments of a digital voltmeter, using the linear staircase approach, without the associated totalizing circuitry.

Fig. 10 shows a block diagram of the system, together with the waveforms of all interfaces. A squelchable integrated-circuit multivibrator is used as the clock. As described later, the clock frequency is independent of supply voltage. Although this independence is not a necessary condition for circuit operation, it is inherent in this type of operational-amplifier multivibrator circuit and may be considered an integrated-circuit bonus.

The output from the clock drives a linear staircase generator. Input voltage to this circuit is applied directly from the multivibrator to minimize the effects of diode temperature coefficients. The output from the staircase generator is applied to a comparator that compares the staircase with the voltage to be measured.

The comparator output fires a monostable multivibrator that controls the display time, which is variable from about 100 milliseconds to one second. An inverter following the multivibrator supplies drive of the correct polarity to the integrator capacitor-discharge switch and the multivibrator squelch circuit.

Circuit operation begins with the staircase generator ramp running down until its voltage is equal to the unknown voltage on the input of the comparator. When the two voltages are equal, the monostable multivibrator is triggered by the output from the comparator. The output of the monostable multivibrator squelches the astable multivibrator and discharges the integrating capacitor through the bistable multivibrator. The wait, or display time, set by the monostable multivibrator allows sufficient time for full discharge of the integration capacitor and appears as a steady reading on the display device.

Astable Multivibrator - A schematic diagram of a squelchable multivibrator is shown in Fig. 11. The only requirement that must be met by the squelch circuit is that the amplitude of the output pulse not change as a result of the squelch operation; otherwise, the amplitude of the final steps would be different from that of the initial steps and staircase linearity would suffer.

Freedom of the circuit from supply-voltage variations results from the excellent saturation characteristics of the integrated circuit at both positive and negative output swings. The positive and negative thresholds of the circuit are given by

$$\text{Positive threshold} = (V_{CC} - V_{CE+sat}) \frac{R_1}{R_1 + R_2}$$

$$\text{Negative threshold} = (V_{EE} + V_{CE-sat}) \frac{R_1}{R_1 + R_2}$$

where V_{CC} and V_{EE} are the positive and negative supply voltages and V_{CE+sat} and V_{CE-sat} are the positive and negative saturation voltages of the amplifier. Be-

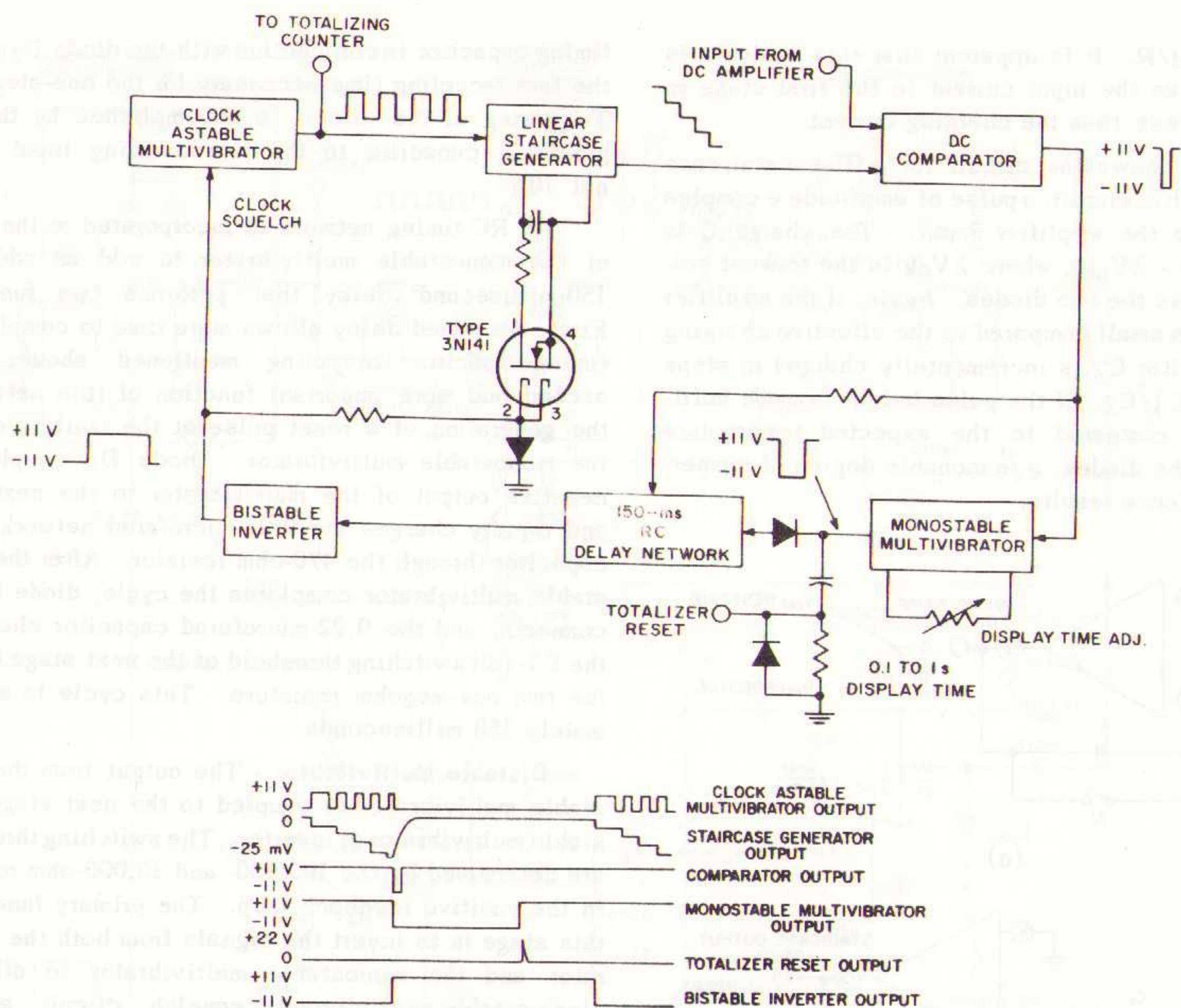


Fig.10 - Block diagram and waveforms of digital voltmeter system using five CA3033 integrated circuits.

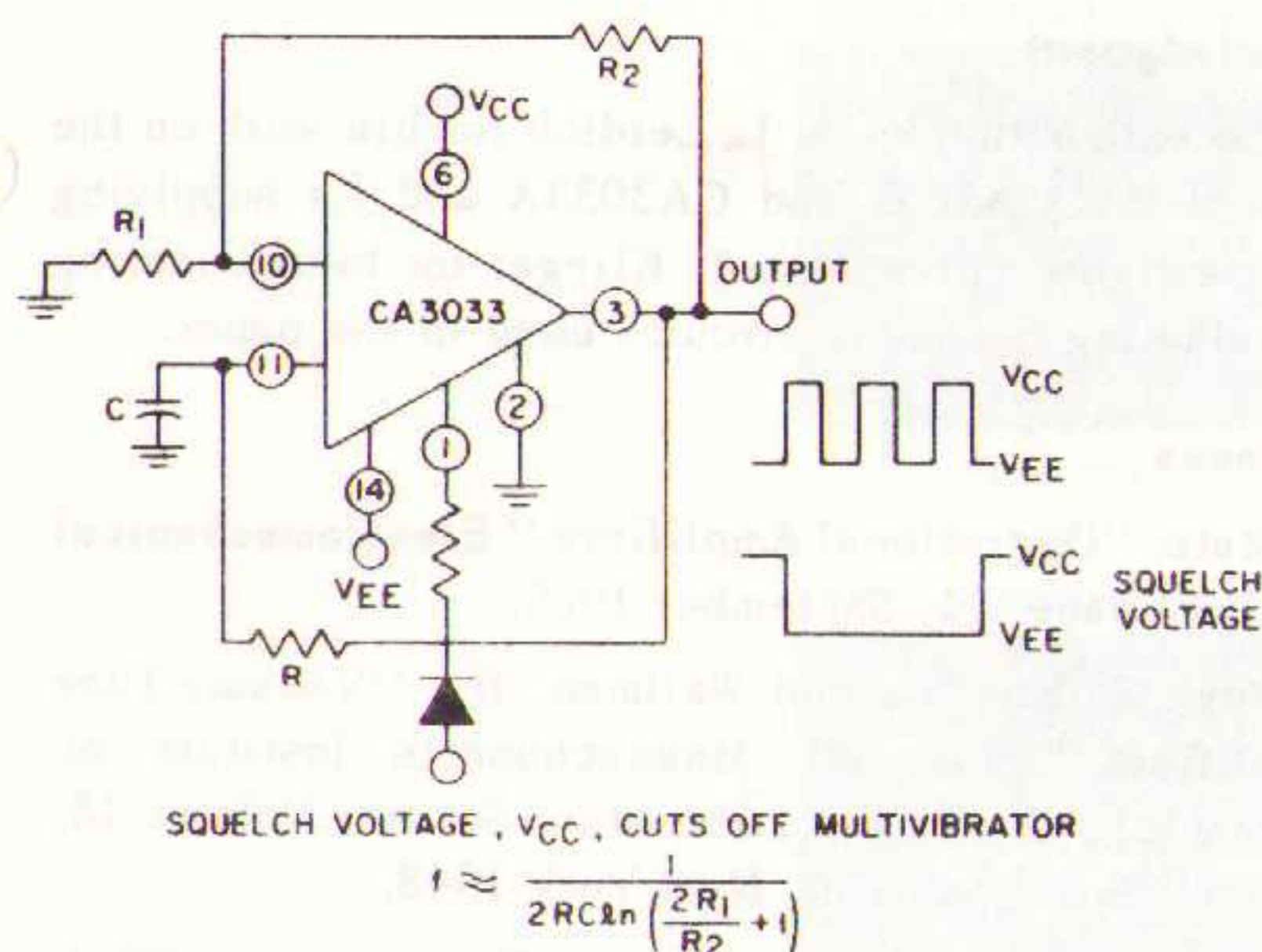


Fig.11 - CA3033 squelchable astable multivibrator.

cause these saturation voltages are low and have temperature coefficients less than 5 millivolts per degree C, they can be neglected for ease of computation. If the charging current is considerably greater than the base current, the frequency f may be expressed as follows:³

$$f \approx \frac{1}{2RC \ln\left(\frac{2R_1}{R_2} + 1\right)}$$

Linear Staircase Generator - The design of a linear staircase generator is nearly identical to that of a linear ramp or sawtooth generator. Fig.12(a) shows a linear ramp generator in which the non-inverting input of an operational amplifier is grounded and a switch S_1 returns the output to the inverting input. When S_1 is closed, the amplifier is in the unity-gain configuration and the output is at ground less the input offset voltage. When S_1 is opened, the output moves in the positive direction when the reference voltage V_{ref} is negative, or in the negative direction when V_{ref} is positive. Because the output under closed-loop conditions tries to maintain the input terminal at zero voltage, the charging current to the capacitor is constant at a rate of $dV/dt = i/C$,

where $i = V_{ref}/R$. It is apparent that this analysis is valid as long as the input current to the first stage is considerably less than the charging current.

Fig. 12(b) shows the circuit for a linear staircase generator. In this circuit, a pulse of amplitude e couples a charge Q to the amplifier input. The charge Q is equal to $C_1(e - 2V_{ak})$, where $2V_{ak}$ is the forward voltage drop across the two diodes. Again, if the amplifier input current is small compared to the effective charging current, capacitor C_2 is incrementally charged in steps of $(e - 2V_{ak}) C_1/C_2$. If the pulse height is made sufficiently large compared to the expected temperature variations of the diodes, a reasonable degree of temperature independence results.

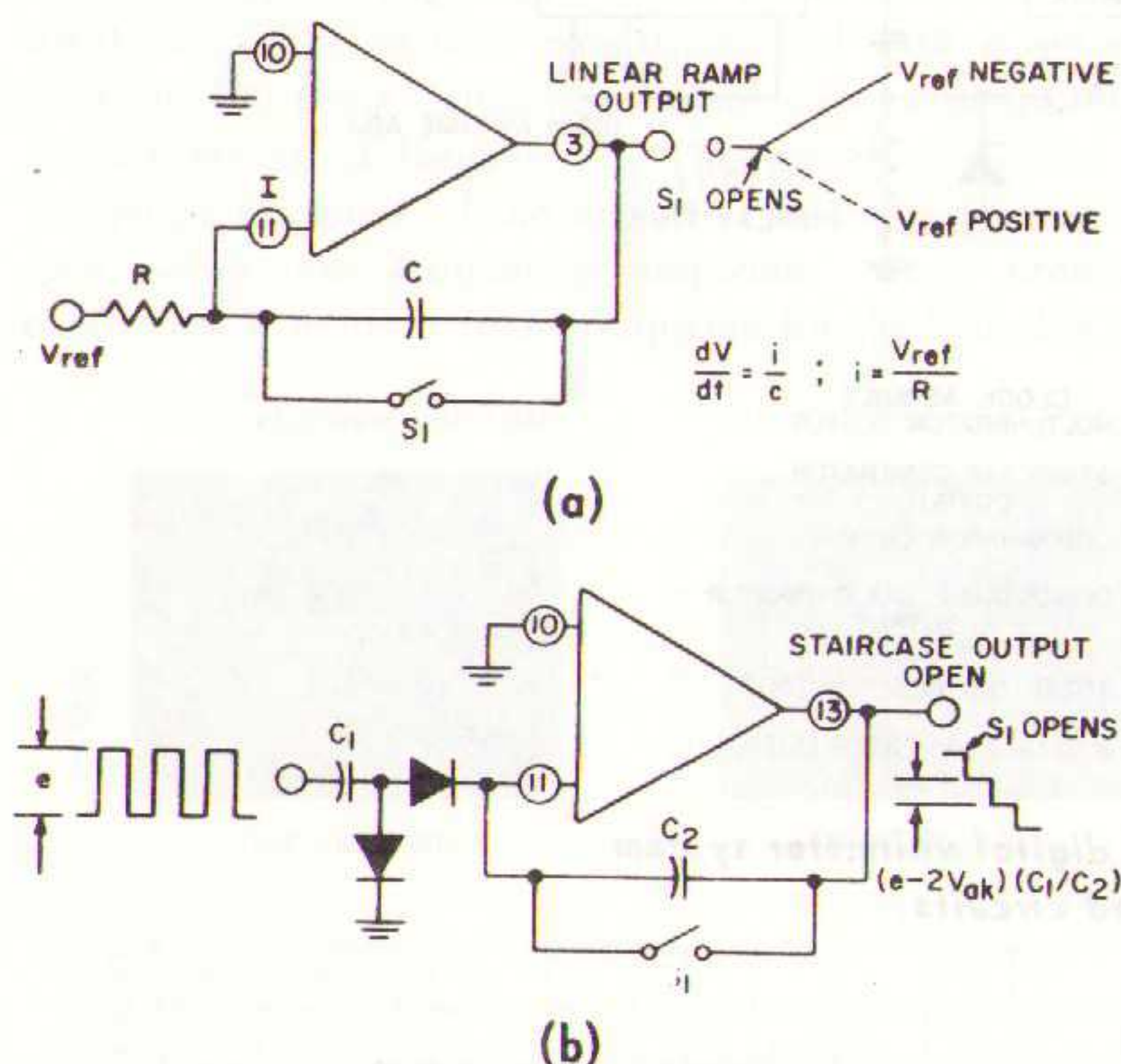


Fig. 12 - Diagrams of (a) linear ramp generator and (b) linear staircase generator.

Comparator - Regeneration is added around the comparator circuit in this system to accelerate the transition time when the two input voltages are equal. Fig. 13 shows a complete schematic diagram of the entire system. Waveforms at critical points are shown in Fig. 14. The 470-picofarad capacitor and 1000-ohm resistor between terminals 3 and 10 of the CA3033 in the comparator circuit provide the regeneration. Two 0.001-microfarad capacitors on each input filter any externally generated noise.

Monostable Multivibrator - The monostable multivibrator circuit shown in Fig. 13 makes use of the extremely low input bias currents of the CA3033 by using small timing capacitors and large timing resistors to obtain the long (one-second) display time. The small

timing capacitor in conjunction with the diode D_3 permits the fast recycling time necessary for the one-step case. Triggering of the circuit is accomplished by the 470-picofarad capacitor to the non-inverting input (terminal 10).

An RC timing network is incorporated at the output of the monostable multivibrator to add an additional 150-millisecond delay that performs two functions. First, the added delay allows more time to complete the timing-capacitor recycling mentioned above. The second and more important function of this network is the generation of a reset pulse at the trailing edge of the monostable multivibrator. Diode D_4 couples the negative output of the multivibrator to the next stage and rapidly charges the 0.22-microfarad network timing capacitor through the 470-ohm resistor. After the monostable multivibrator completes the cycle, diode D_4 disconnects, and the 0.22-microfarad capacitor charges to the 1.1-volt switching threshold of the next stage through the two one-megohm resistors. This cycle is approximately 150 milliseconds.

Bistable Multivibrator - The output from the monostable multivibrator is coupled to the next stage, a bistable multivibrator or inverter. The switching thresholds are determined by the 100,000- and 10,000-ohm resistors in the positive feedback loop. The primary function of this stage is to invert the signals from both the comparator and the monostable multivibrator to drive the clock-astable-multivibrator squelch circuit and the staircase capacitor-discharge switch, an RCA-3N141 dual-gate MOS field-effect transistor. Diode D_6 protects the gates of the MOS transistor; the 47-picofarad capacitor reduces the rise time of the negative-going output of the bistable multivibrator and prevents it from coupling into the beginning of staircase and obscuring the first few steps by this negative transition.

Acknowledgment

The author thanks A. J. Leidich for his work on the design of the CA3033 and CA3033A and for supplying the noise-figure curve, and J. Klinger for breadboarding and evaluating the many circuits used in the paper.

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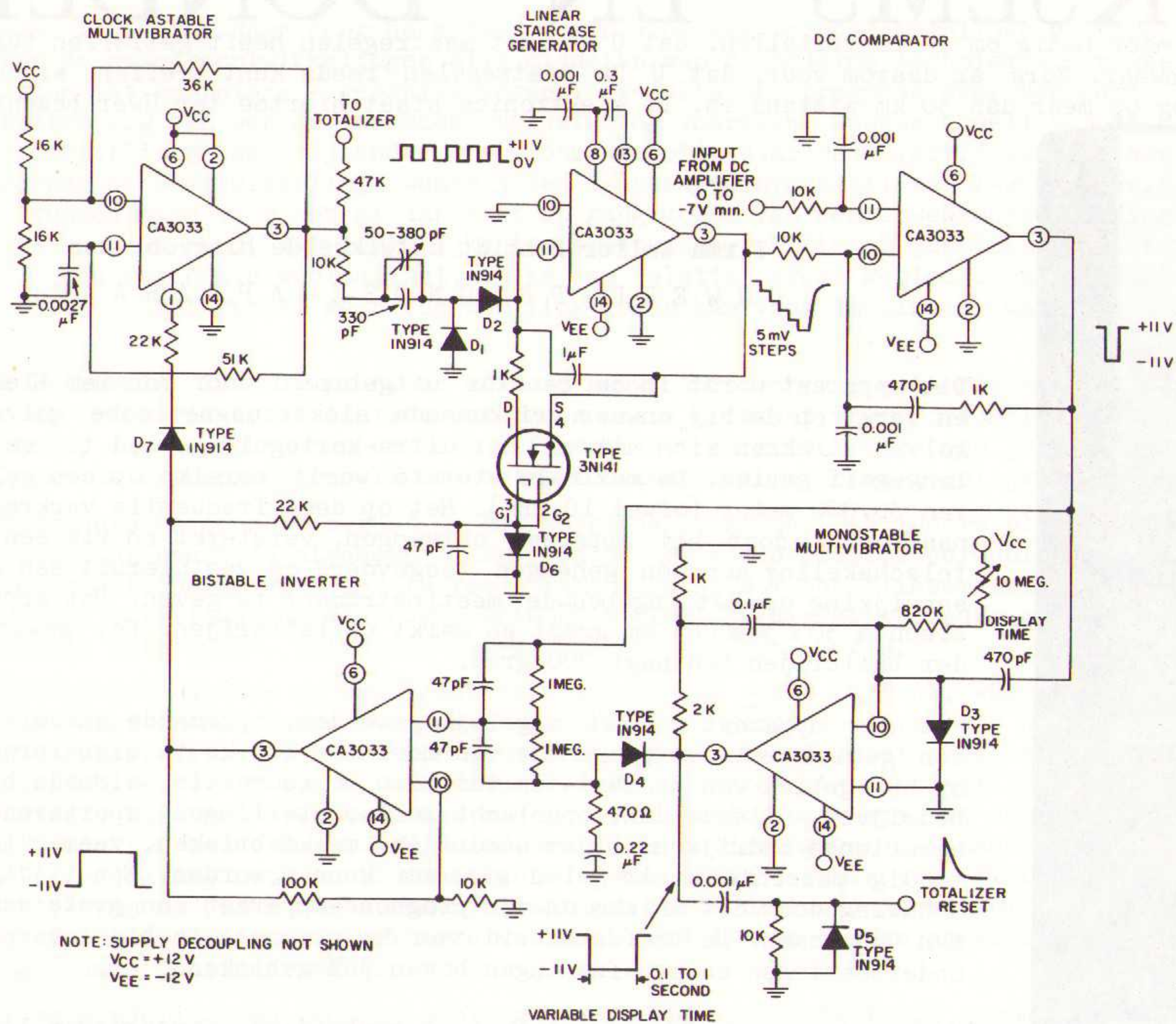


Fig.13 - Schematic diagram of a digital voltmeter using CA3033 integrated circuits.

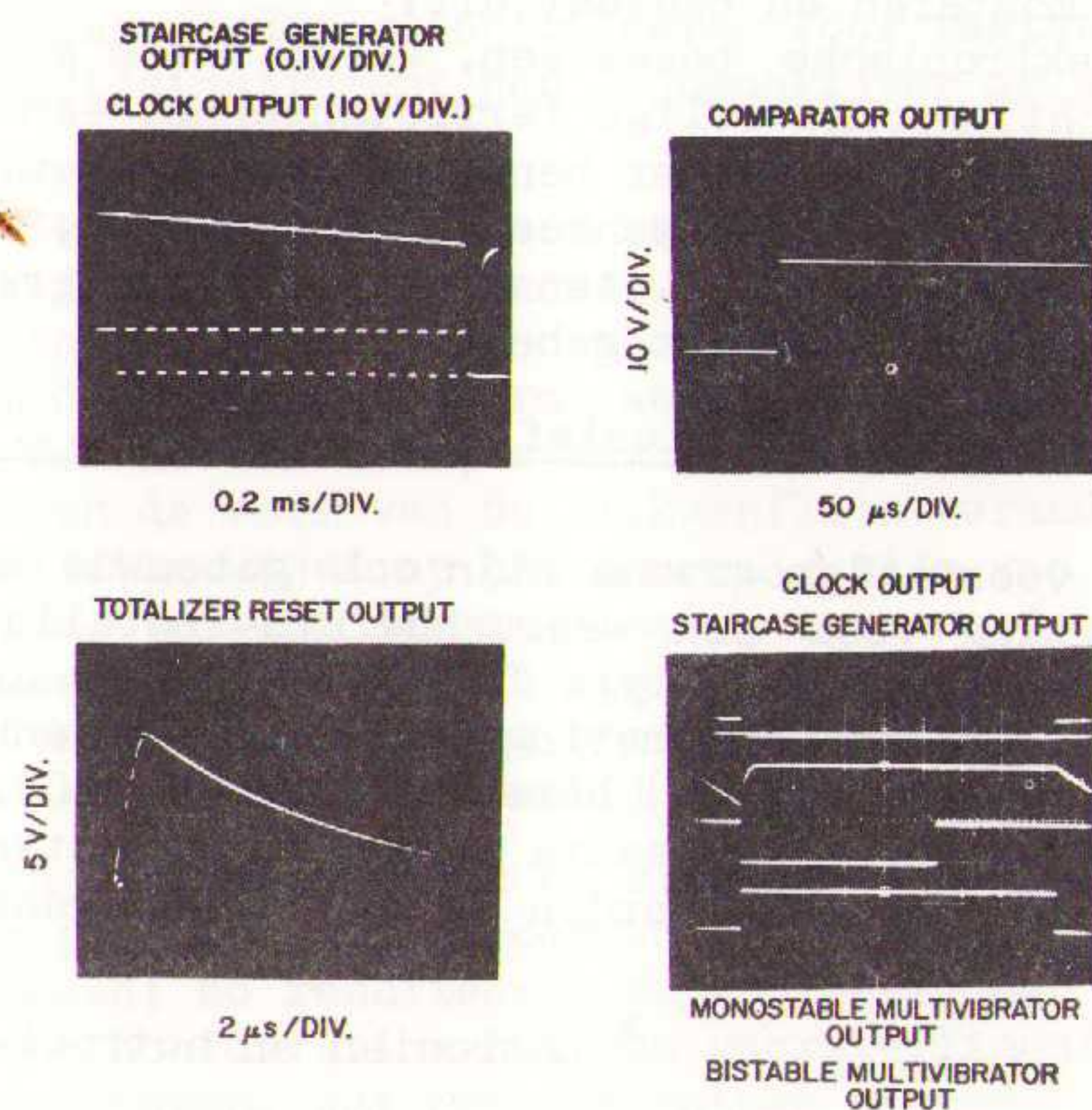
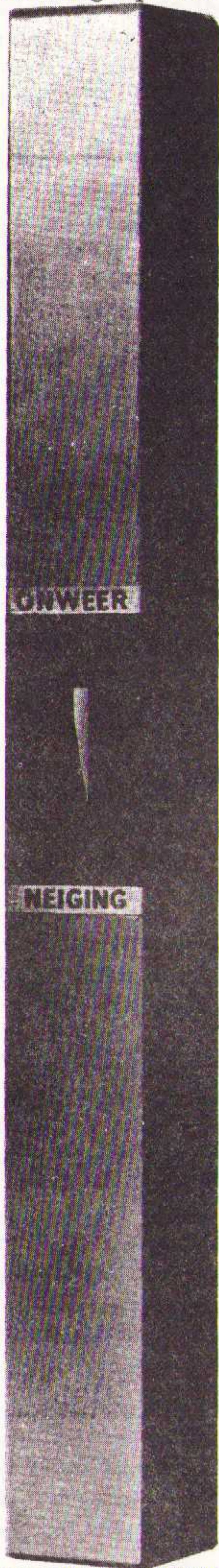


Fig.14 - Waveforms for the digital voltmeter shown in Fig.13.

BLIKSEMS EN DONDERS

zijn niet meer nodig om U te vertellen, dat U te laat maatregelen heeft getroffen tegen een naderend onweer. Zorg er daarom voor, dat U Uw maatregelen reeds kunt treffen, als een onweersbui nog op meer dan 30 km afstand is. De elektronica staat hiertoe ter Uwer beschikking.



Firma Walter Schmidt ontwikkelde hiervoor een
ONWEER - PROGNOSE - APPARAAT

Dit apparaat wordt in de Benelux uitgebracht door Van Dam Elektronica en werkt op de bij onweer vrijkomende elektromagnetische golven. Deze golven strekken zich uit van het ultra-kortegolf gebied tot ver in het langegolf gebied. De maximale sterkte wordt bereikt op een golflengte van 30.000 meter (ofwel 10 kHz). Het op deze frequentie verkregen signaal wordt door het apparaat ontvangen, versterkt en via een analoge telschakeling aan een geheugen toegevoerd om van hieruit een continue aanwijzing op het ingebouwde meetinstrument te geven. Het apparaat is slechts 30 x 30 x 285 mm groot en werkt op batterijen. Het gewicht zonder batterijen bedraagt 200 gram.

Met dit apparaat is het mogelijk geworden, opkomende onweersbuien in een gebied met een doorsnede van meer dan 100 km te signaleren, zodat op het gebied van de land- en tuinbouw en recreatie, alsmede bij bouwbedrijven, vliegvelden, openlucht tentoonstellingen, sportevenementen, agrarische bedrijven, bloemkwekerijen, melkfabrieken, veemarkten, enz. tijdig passende maatregelen genomen kunnen worden. Een tijdige waarschuwing door dit unieke onweer-prognose-apparaat kan grote schadekosten voorkomen. De trefzekerheid van de prognose is bij internationale onderzoeken en proefnemingen boven 90% gebleken!

Het hier besproken apparaat is in verscheidene uitvoeringen leverbaar. Als bouwpakket wordt het type THP 800 K geleverd. Dit pakket is eenvoudig te monteren en bestaat uit:

een elektronische bouwsteen, welke reeds gemonteerd en afgeregeld is, een richtingsongevoelige ferrietantenne, een trommel-aanwijsinstrument van 100 μ A en de verder benodigde materialen, zoals kast, lijm, draad, soldeer, schakelaar, schroeven, enz., enz., alsmede een gedetailleerde bouwbeschrijving met wetenschappelijke gegevens over het ontstaan van een onweersbui met het gehele verloop.

PRIJS bouwpakket exclusief 14% B.T.W. f 103,50 (Bfr. 1475,-).

In het voorraadprogramma zijn ook gebouwde uitvoeringen met een extra aansluiting voor een waarschuwings-installatie of een registrerende schrijver opgenomen (type THP 800S) en een uitvoering met een tweevoudig meetsysteem voor meting in relatieve eenheden in een nabij (30 km) en een veraf (250 km) bereik (type THP 200). Op deze laatste uitvoering zijn voornoemde extra aansluitingen standaard aangebracht. Nadere gegevens en prijzen worden U op aanvraag gaarne verstrekt.

* Octrooien en octrooi-aanvragen in vele landen.

VAN DAM
ELEKTRONICA

Alleenvertegenwoordiger voor de Benelux landen:
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Een elektronisch apparaat voor onweersvoorspelling.

Hoewel heden ten dage door de meteorologen voor een zo goed mogelijke voorspelling van de onweersontwikkelingen alle middelen van de moderne techniek - van weersatellieten tot computers - gebruikt worden, is zelfs een prognose over een kort tijdsbestek nog van een grote onzekerheidsfactor voorzien. Onweer speelt bij de weersvoorspellingen een bijzonder grote onzekerheid, daar het hierbij gaat om een thermodynamische ontwikkeling, waarbij een temperatuursverschil van 1-2°C doorslaggevens kunnen zijn voor het al dan niet op gang komen van een onweersontwikkeling. Het ligt voor de hand, dat dergelijke temperatuursverschillen bijzonder lokaal zijn, waardoor een regionale weersdienst, welke een relatief groot gebied bestrijkt, in vele gevallen in het geheel geen voorspelling geven kan voor de plaats, waar U zich bevindt.

Met betrekking tot dit probleem werd in nauwe samenwerking met onderzoekingscentra en de industrie in de laatste jaren een klein apparaat voor produktiedoeleinden ontwikkeld, dat de vakman en de leek informatie verschafft, welke een juiste beoordeling van de onweersneiging in het betrokken waarnemingsgebied mogelijk maakt.

Het technische concept berust op het volgende principe. Bij iedere bliksemontlading ontstaan, naast de algemeen bekende optische en akoestische verschijnselen, ook elektromagnetische golven. Het is reeds lang bekend, dat een bliksemstraal in zekere zin een tot trillingen aangespoorde antenne voorstelt, die kortstondig een impulsvormig signaal uitstraalt, welke een breed frequentiegebied overlapt.

Deze impulsen worden op een frequentie van 10 kHz $\pm$ 200 Hz/3 dB, waar de maximale amplitude ligt in het beschreven apparaat met een ingebouwde verticale antenne ontvangen en versterkt. Boven een instelbaar amplitude-niveau wordt door iedere impuls een monostabiele multivibrator aangestuurd, die gedurende zijn omslagtijd een bepaalde constante ladingshoeveelheid aan een laadcondensator toevoert. Na deze oplading, die na circa 100 msec. wordt beëindigd, volgt de ontlading van de laadcondensator via de aanwyskring met een tijdconstante τ van circa 4-6 minuten. Evenredig aan de frequentie van de ontvangen bliksemontladingen wordt de laadcondensator met een hogere spanning opgeladen, welke derhalve resulteert in een hogere aanwijswaarde op het ingebouwde meetinstrument.

Ter vermindering van kans op storingen, die bij lichtnetgebruik kunnen optreden, wordt het apparaat gevoed uit twee monocellen, die bij de THP 800, 800K en 800S ongeveer iedere 5-6 maanden moeten worden uitgewisseld. De batterijspanning kan door middel van een proefschakelaar worden gecontroleerd. Voor registratie van de meetwaarde kan in serie met het aanwysinstrument een lijnschrijver of een puntdrukker aangesloten worden.

Zoals gezegd, stelt de aanwijswaarde een maatstaf voor van de hoeveelheid geregistreerde veraf en dichtbij opgetrede bliksems, waarbij de gevoeligheid zó gekozen is, dat bliksemontladingen in een gebied van circa 100 km doorsnede ontvangen worden. Dat er hier slechts een gemiddelde waarde wordt weergegeven ligt aan de grote verscheidenheid in intensiteit van de bliksems, evenals aan de verschillende stralingscondities, die met de lengte en de vorm van de bliksenflits veranderen. Het kan daarom zijn, dat een lage aanwijzing wijst op het aanwezig zijn van een enkele onweersbui in het betreffende gebied, terwijl een regelmatig toenemende aanwijzing bijvoorbeeld de nadering van een onweersfront aangeeft. Op grond van deze informatie is een voorspelling over de graad van onweersneiging voor het meetgebied, resp. de waarschijnlijkheidsfactor voor de vorming van een nabij onweer mogelijk.

Nadat het gebruik van registratie van de bliksemfrequenties door verschillende auteurs (5) en (6) zeer positief werd beoordeeld, gaven ook deze apparatuur een hoge graad van prognosezekerheid; zo resulteerde bijvoorbeeld een testserie door het Zwitserse meteorologische hoofdstation bij een voorspellingstijd van 1-6 uur bij 53 gevallen in 48 juiste prognosen, wat een percentage van meer dan 95% betekent. Zonder twijfel is de juistheid van de prognose afhankelijk van de plaatselijke klimatologische omstandigheden, het niet van invloed zijn van storingen door nevenapparatuur en, niet te vergeten, ook de ervaring van de waarnemer, waarmee de informatie van deze apparatuur op de juiste wijze kan worden uitgelegd.

Voor literatuurlijst zie volgende pagina.

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22-1-1970.

Dr. Heinz-Jürgen Fischer, Dipl.-Physiker
Ravensburg - West-Duitsland

- - - - -

Voor verdere gegevens van deze onweer-prgnose-apparatuur, waarvan wij sinds maart j.l. de Benelux vertegenwoordiger zijn, verwijzen wij U naar de maart-advertenties in Radio Bulletin en Radio Elektronica, de april-advertentie in Elektuur, de mei-advertentie in Landbouwmecanisatie en de binnenkort in de dag- en vakbladen verschijnende rapporten over deze unieke apparatuur.

- - - - -

VOIN DAM
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heeft free-lance werk; ook voor U !

Onze activiteiten blijven nog steeds toenemen. Daartoe hebben wij niet alleen medewerkers in vaste dienst nodig, doch ook free-lance medewerkers, die bereid zijn tegen een passende vergoeding research en tekenwerk (o.a. printen ontwerpen) voor hun rekening te nemen. Wij denken daarbij vooral aan studenten, welke in de avonduren nog tijd hebben, om voornoemde activiteiten te ontplooiën.

Bent U geïnteresseerd in free-lance werk? Geeft U dan Uw naam en adres aan ons op: zodra wij passend werk voor U hebben, nemen wij contact met U op. Geeft U op Uw aanmelding ook even Uw voorkeur aan?

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Rotterdam-N

RCA CA3059*zero-voltage switch is a monolithic silicon integrated circuit designed to control a thyristor in a variety of ac power switching applications.

The zero-voltage switch consists of the following four major functional blocks (See Fig. 1):

1. Limiter-Power Supply – Permits operation directly from an ac line.
2. Differential On/Off Sensing Amplifier – Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector – Synchronizes the output pulses of the circuit with the time of zero-voltage in the ac cycle to eliminate radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit – Provides high-current pulses to the gate of the power controlling thyristor.

In Addition, the CA3059 also provides the following important auxiliary functions:

1. A built-in protection circuit which may be connected to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

An explanation of these functions is given in the Operating Considerations Section of this data bulletin.

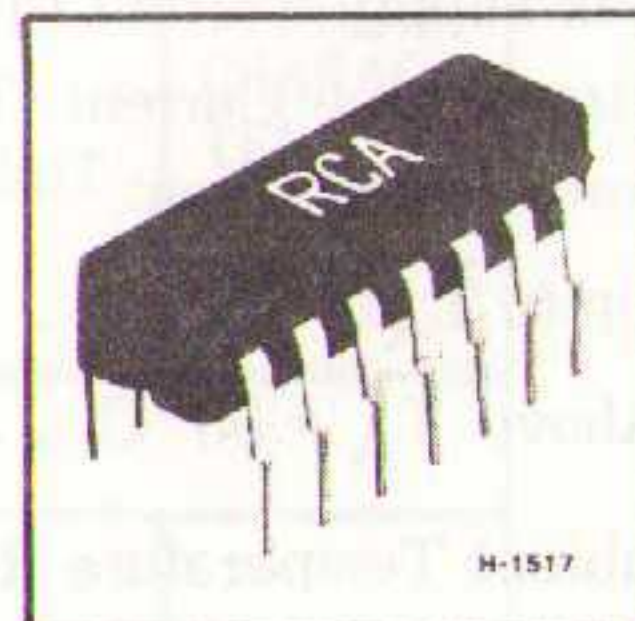
For detailed application information, see companion Application Note, ICAN 4158 "Applications of the CA3059 Zero-Voltage Switch in Thyristor Circuits".

The CA3059 is supplied in a 14-lead dual-in-line plastic package and is designed to operate over the temperature range of -40°C to $+85^{\circ}\text{C}$.

*Formerly TA5615A

ZERO-VOLTAGE SWITCH

50 to 400 Hz Thyristor Control Applications



APPLICATIONS

- Relay control
- Heater control
- Valve control
- Lamp control
- Photosensitive control
- Synchronous switching of flashing lights
- Power one-shot control
- On-off motor switching
- Differential comparator for industrial applications

FEATURES

- Differential input
- 120 V line operation at 50 Hz, 60 Hz, or 400 Hz
- Low balance input current -- 500 nA max.
- High peak output current (pulsing) -- 90mA min.
- Low peak output leakage current (inhibit) -- $10\mu\text{A}$ max.
- Flexible connection arrangement permits:
 - Application of positive feedback for increased circuit hysteresis
 - Application of proportional control for precise temperature control operation with inductive loads
- Self-contained power supply to supply dc bias current for external components
- Built-in protection circuit for opened or shorted sensor
- Typically sensitive to 1% change when Sensor resistance = $5\text{ k}\Omega$, and to 3% change when Sensor resistance = $100\text{ k}\Omega$

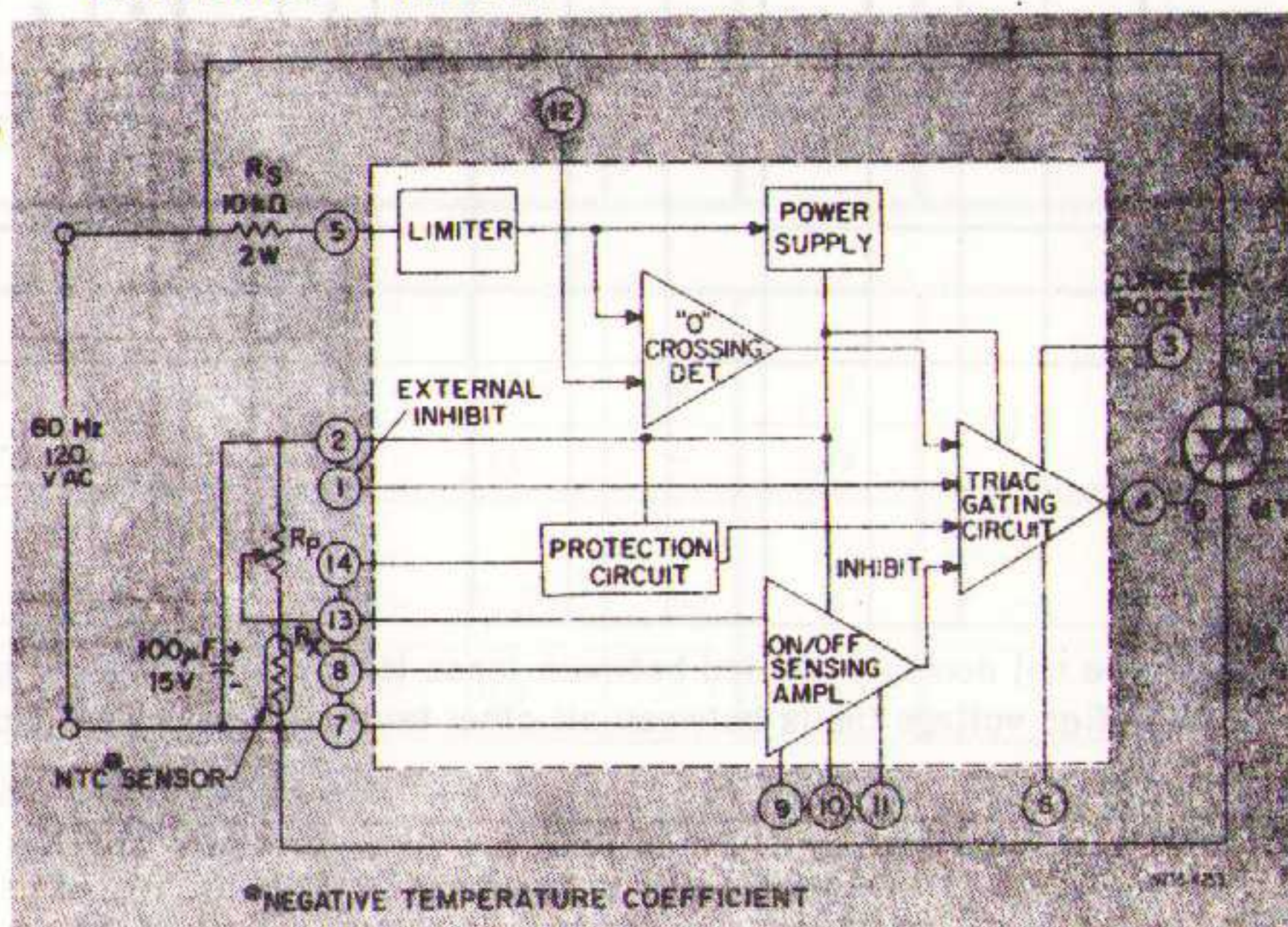


Fig. 1 - Functional block diagram

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, at $T_A = 25^\circ\text{C}$

DC Supply Voltage (between Terminals 2 and 7)	14	V
DC Supply Voltage (between Terminals 2 and 8)	14	V
Peak Supply Current (Terminals 5 and 7)	± 50	mA
Output Pulse Current (Terminal 4)	150	mA
Power Dissipation:		
Up to $T_A = 55^\circ\text{C}$	700	mW
Above $T_A = 55^\circ\text{C}$	Derate linearly 6.67	mW/ $^\circ\text{C}$
Ambient Temperature Range:		
Operating	- 40 to + 85	$^\circ\text{C}$
Storage	- 65 to + 150	$^\circ\text{C}$

MAXIMUM VOLTAGE RATINGS at $T_A = 25^\circ\text{C}$

TERM- INAL NO.	1	2	3	4	5 NOTE 1	6	7	8	9	10	11	12	13	14 NOTE 2	This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.		I _{IN} mA	I _{OUT} mA
1		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*			10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 -14	0 -14	0 -14	0 -14	0 -14	*	0 -14	0 -14			150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*			*	*
4					*	2 -10	*	*	*	*	*	*	*	*			0.1	150
5 NOTE 1						*	7 -7	*	*	*	*	*	*	*			50	10
6							14 0	*	*	*	*	*	*	*			*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6			*	*
8									10 0	*	*	*	*	*			0.1	2
9										*	*	*	*	*			*	*
10											*	*	*	*			*	*
11												*	*	*			*	*
12													*	*			50	50
13														*			*	*
14																	2	2

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2 mA.

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2 mA.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	SPECIAL TEST CONDITIONS	LIMITS			UNIT	TYPICAL CHARAC- TERISTICS CURVE
		Fig. No.		Min.	Typ.	Max.		Fig. No.
For Operation at 120 V rms, 50-60 Hz (AC Line Voltage)								
DC Supply Voltage: Inhibit Mode	V_S	3a	$R_S = 10\text{ k}\Omega$	6.1	6.5	7	V	3b
Pulse Mode	V_S	3a	$I_L = 0$	6	6.4	7	V	3b
DC Supply Voltage: Inhibit Mode	V_S	3a	$R_S = 5\text{ k}\Omega$	—	6.4	—	V	3c
Pulse Mode	V_S	3a	$I_L = 2\text{ mA}$	—	6.3	—	V	3c
Peak Output Current (Pulsed) With Internal Power Supply	$I_{OM(4)}$	5a	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	—	mA	5b
			Term. 3 connected to Term. 2, Gate Trigger Voltage (V_{GT}) = 0	90	124	—	mA	5b
Peak Output Current (Pulsed) With External Power Supply	$I_{OM(4)}$	6a	Term. 3 open, $V_{CC} = 12\text{ V}$, $V_{GT} = 0$	—	170	—	mA	6b, c
			Term. 3 connected to Term. 2, $V_{CC} = 12\text{ V}$, $V_{GT} = 0$	—	240	—	mA	6b, c
Gate Trigger Current	$I_{GT(4)}$	5a	Term. 3 connected to Term. 2, $V_{GT} = 1\text{ V}$	—	105	—	mA	4
Output Leakage Current Inhibit Mode	I_4	—	—	—	—	10	μA	7
Input Bias Current	I_1	8	—	—	220	1000	nA	—
Inhibit Input Ratio	V_9/V_2	9a	Voltage Ratio of Term. 9 to Term. 2	0.465	0.485	0.520	—	9b
Total Gate Pulse Duration:*			External Capacitance					
For positive dv/dt	t_p	10 a, b	$C_{(EXT)} = 0$	70	100	140	μs	10 c
For negative dv/dt	t_N	10 a, b	$R = \infty$	70	100	140	μs	10 c
Pulse Duration (After Zero Crossing):								
For positive dv/dt	t_{p1}	10 a, b	$C_{(EXT)} = 0$	—	50	—	μs	10 d
For negative dv/dt	t_{N1}	10 a, b	$R = \infty$	—	60	—	μs	10 d
For Operation at 120 V rms, 400 Hz								
Total Gate Pulse Duration:								
For positive dv/dt	t_p	10 a	$C_{(EXT)} = 0$	—	12	—	μs	10 e
For negative dv/dt	t_p	10 a		—	11	—	μs	
DC Supply Voltage:								
Inhibit Mode	V_S	3a	$R_S = 10\text{ k}\Omega$, $I_L = 0$	—	6.8	—	V	—
Pulse Mode	V_S	3a	$R_S = 10\text{ k}\Omega$, $I_L = 0$	—	6.7	—	V	—

*Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 10 b.

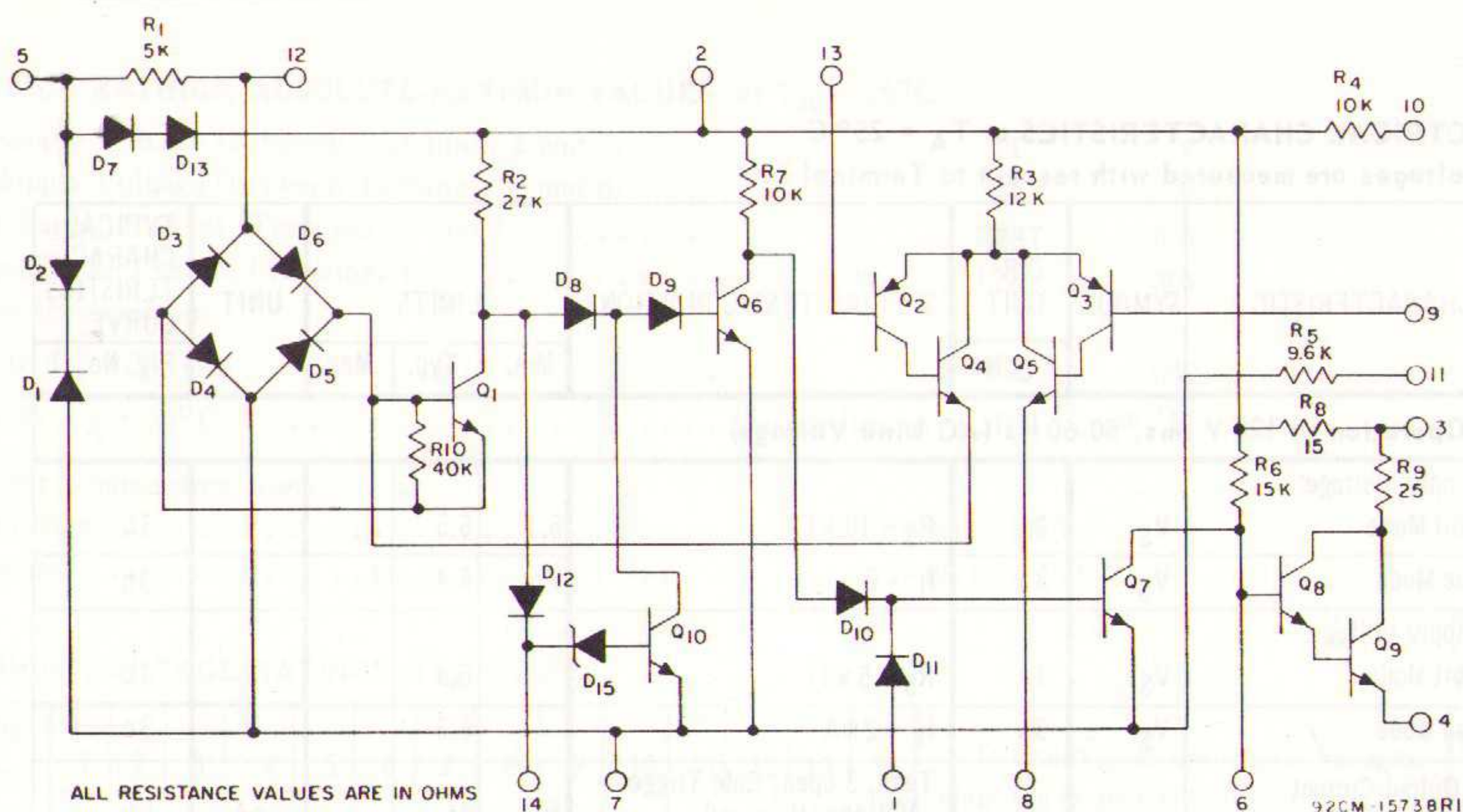


Fig. 2 - Schematic diagram for CA3059

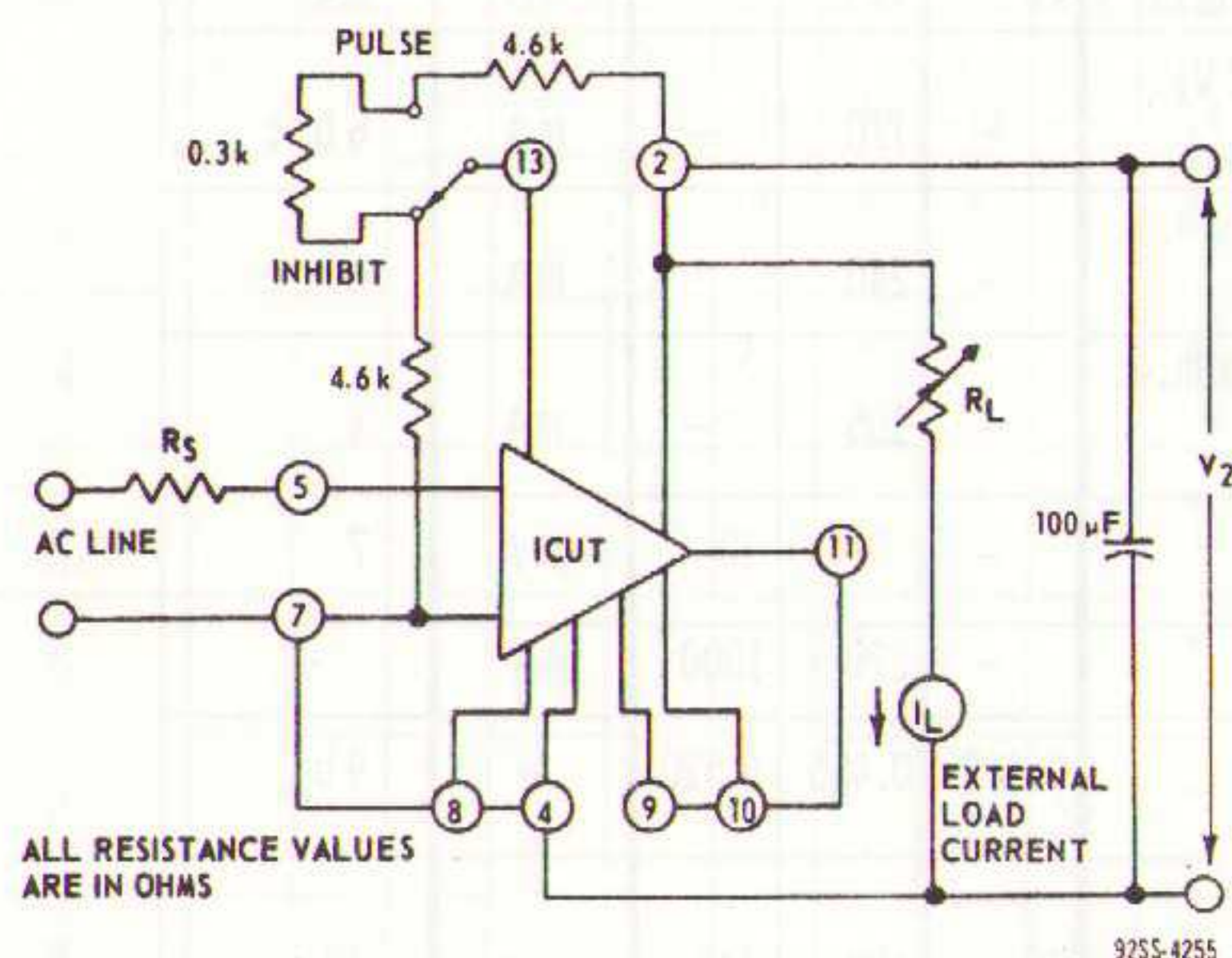


Fig. 3a - DC supply voltage test circuit

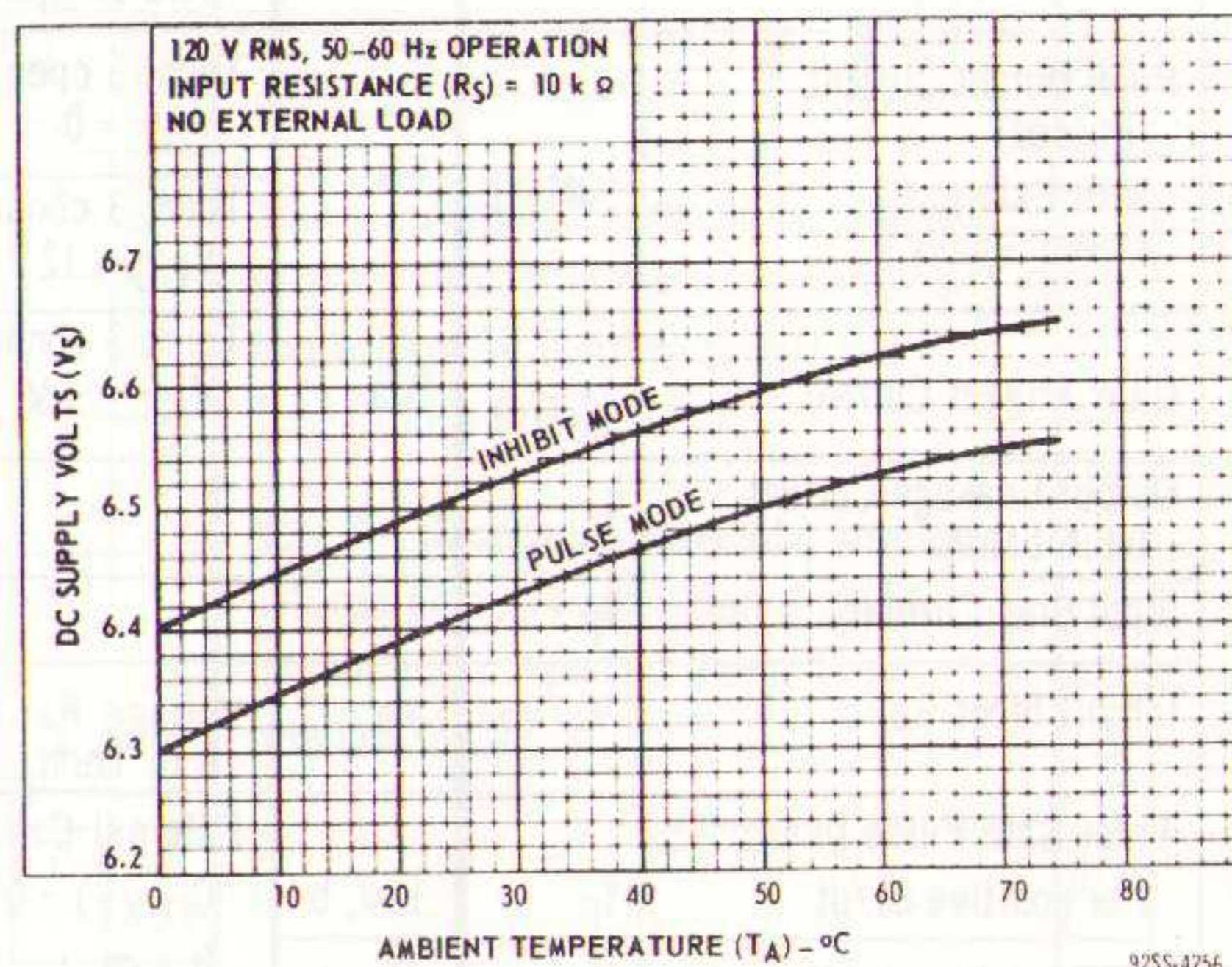


Fig. 3b - DC supply voltage vs. ambient temperature

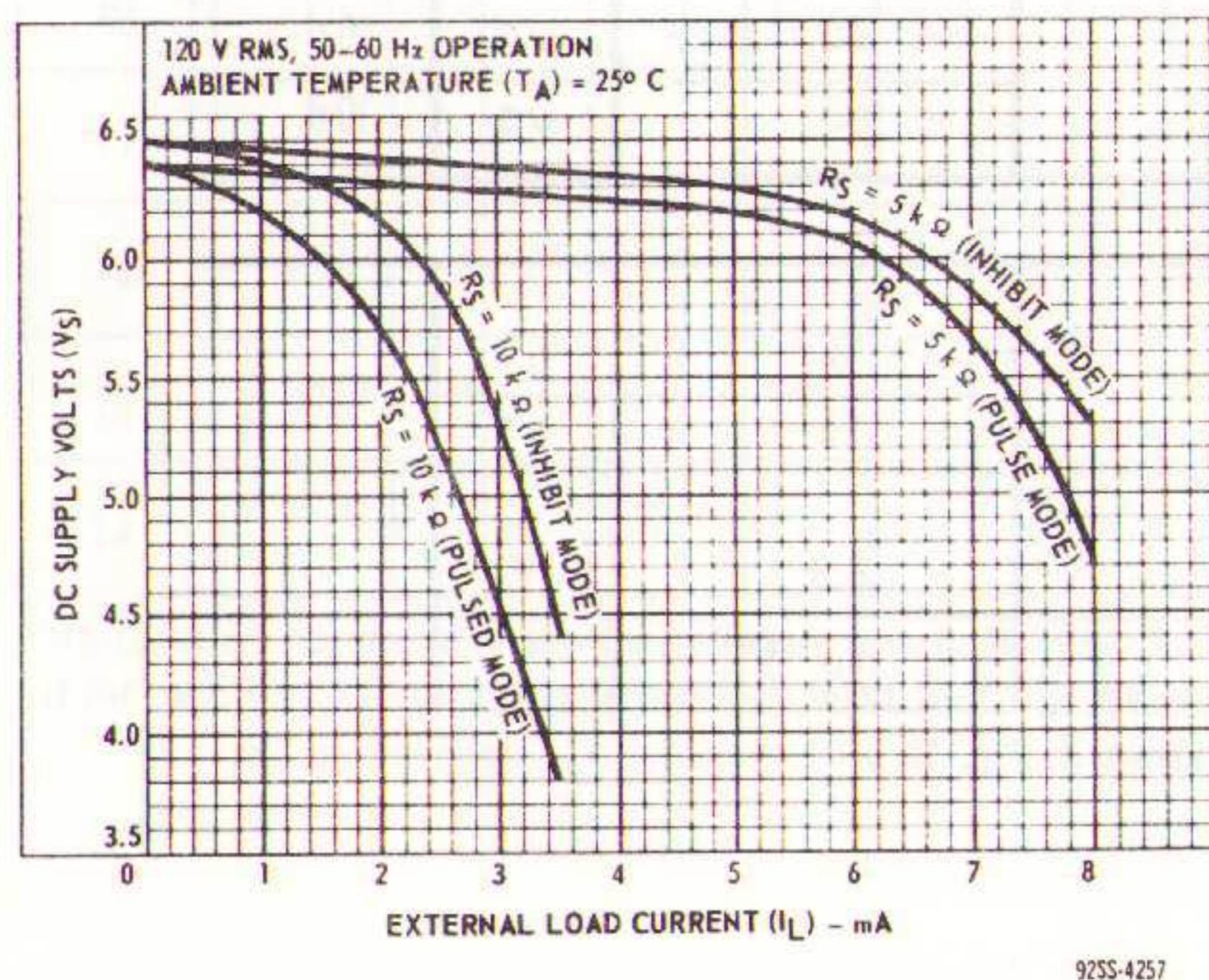


Fig. 3c - DC supply voltage vs. external load current

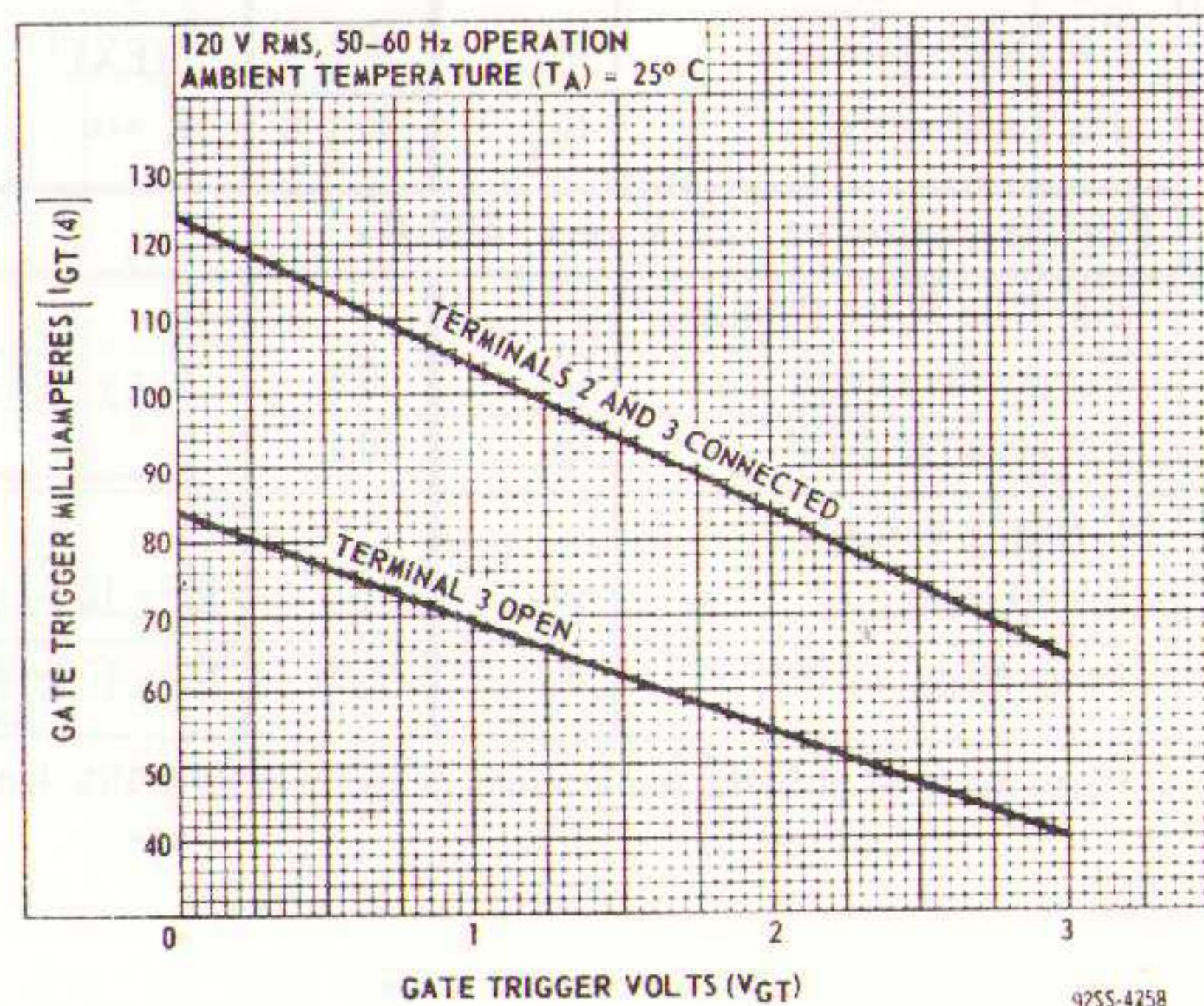


Fig. 4 - Gate trigger current vs. gate trigger voltage

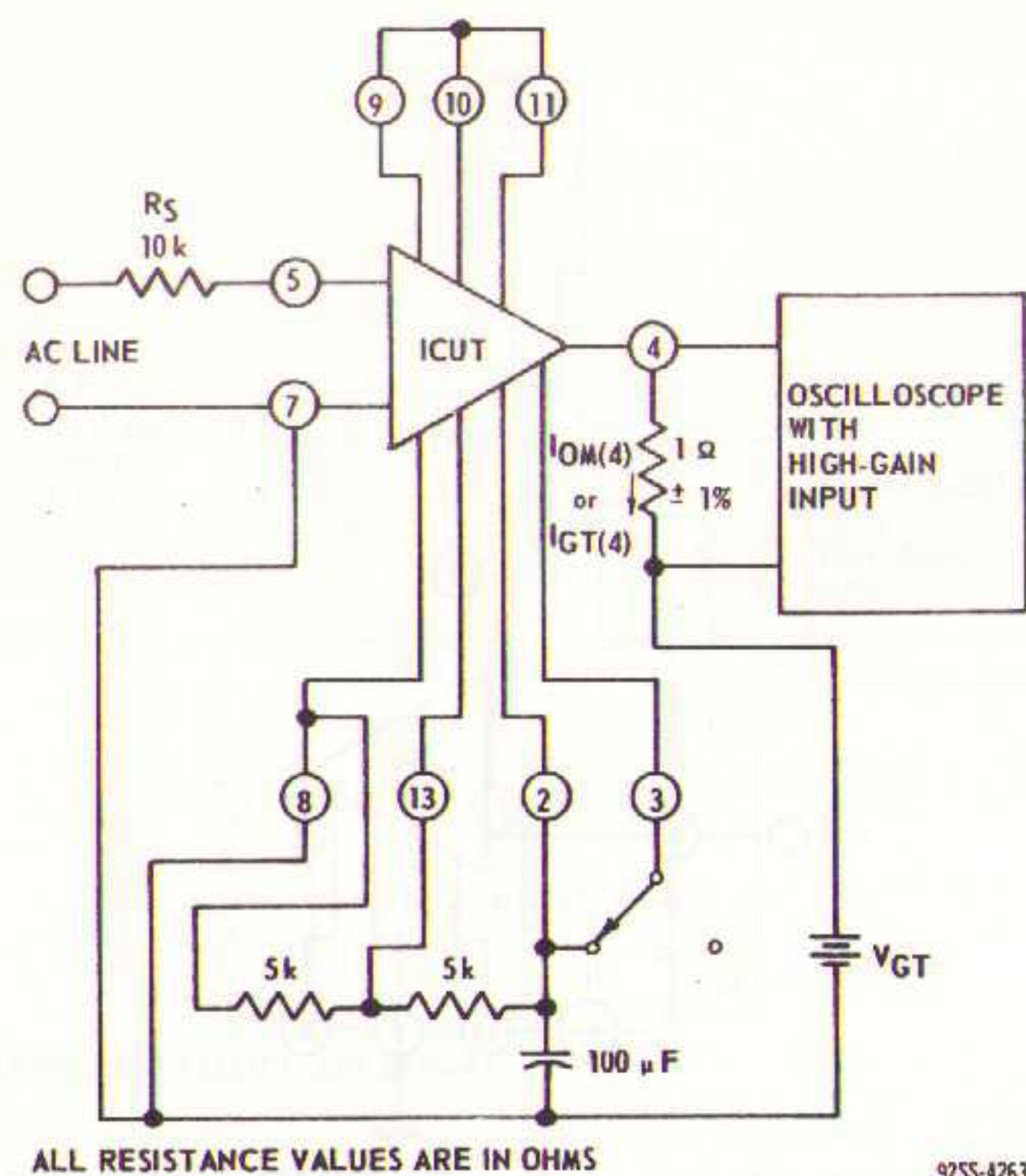


Fig. 5a - Peak output (pulsed) and gate trigger current with internal power supply test circuit

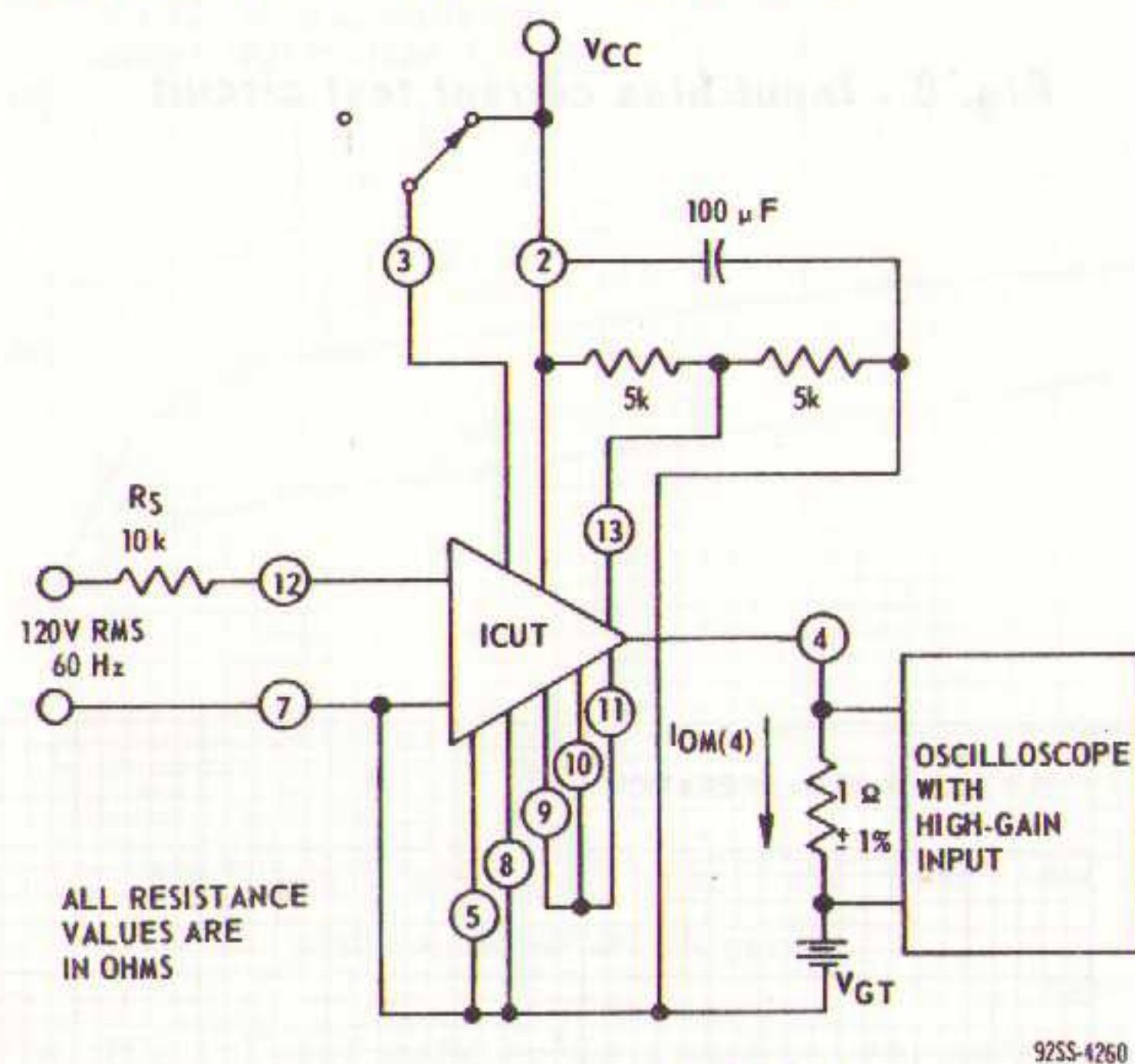


Fig. 6a - Peak output current (pulsed) with external power supply test circuit

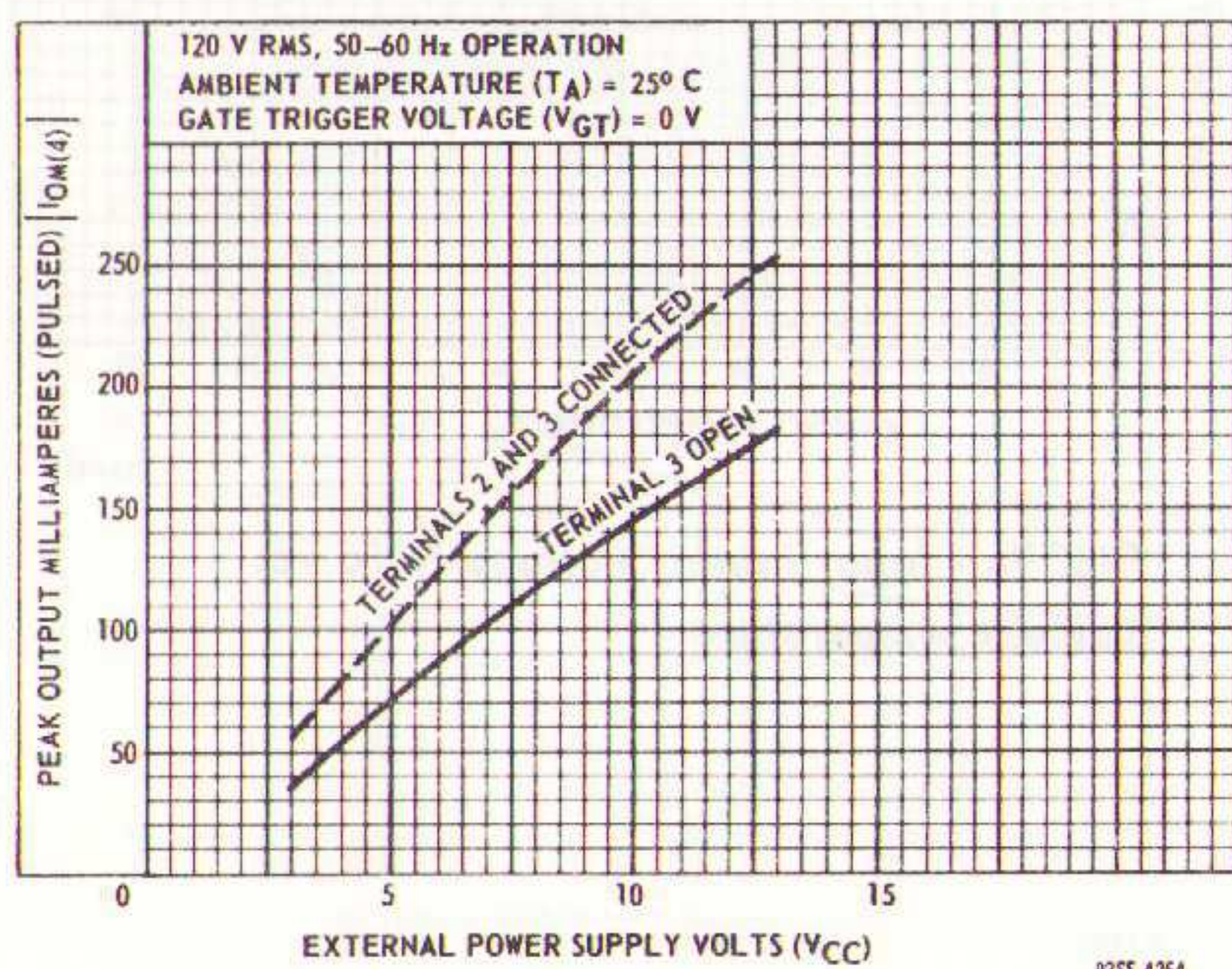


Fig. 6b - Peak output current (pulsed) vs. external power supply voltage

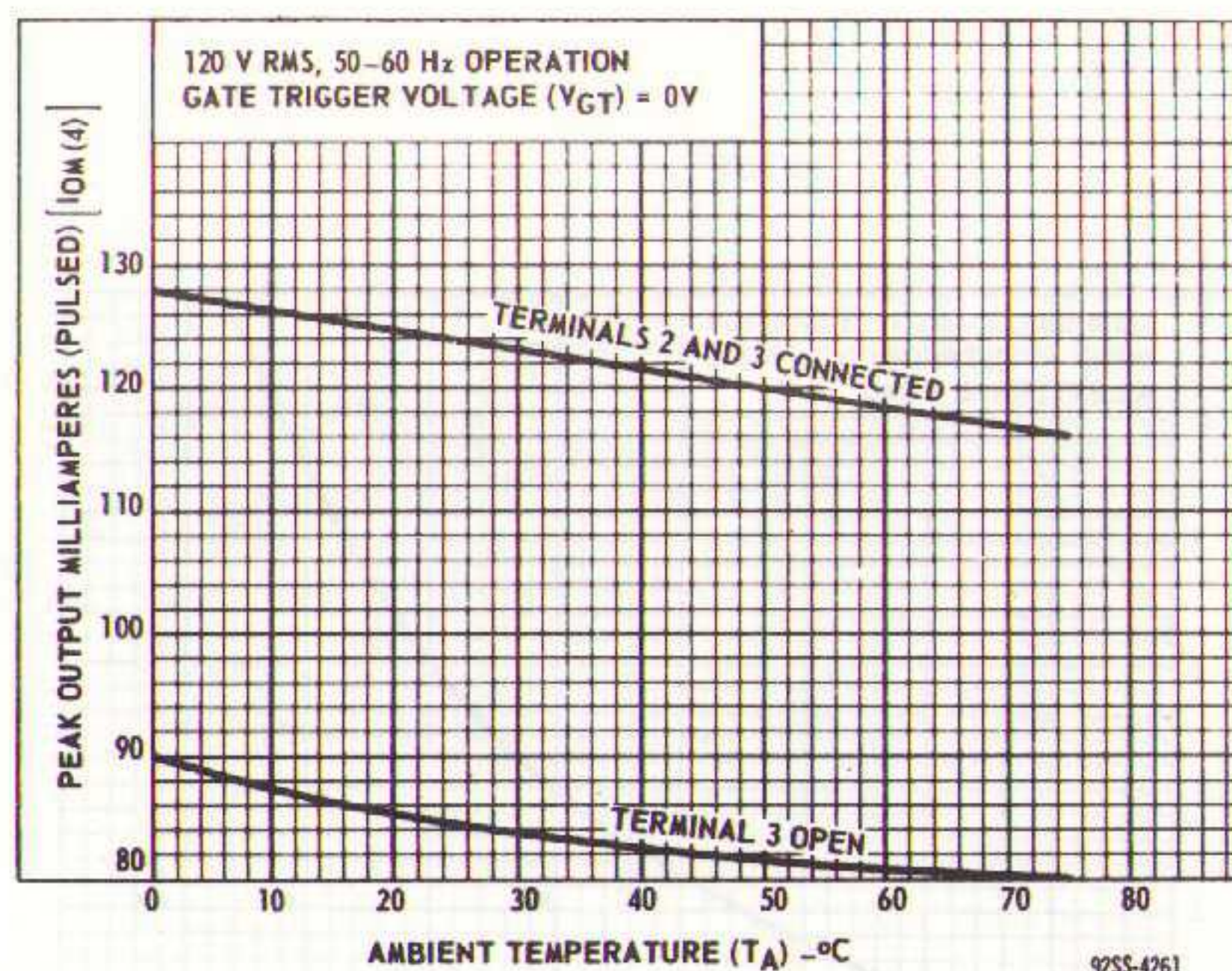


Fig. 5b - Peak output current (pulsed) vs. ambient temperature

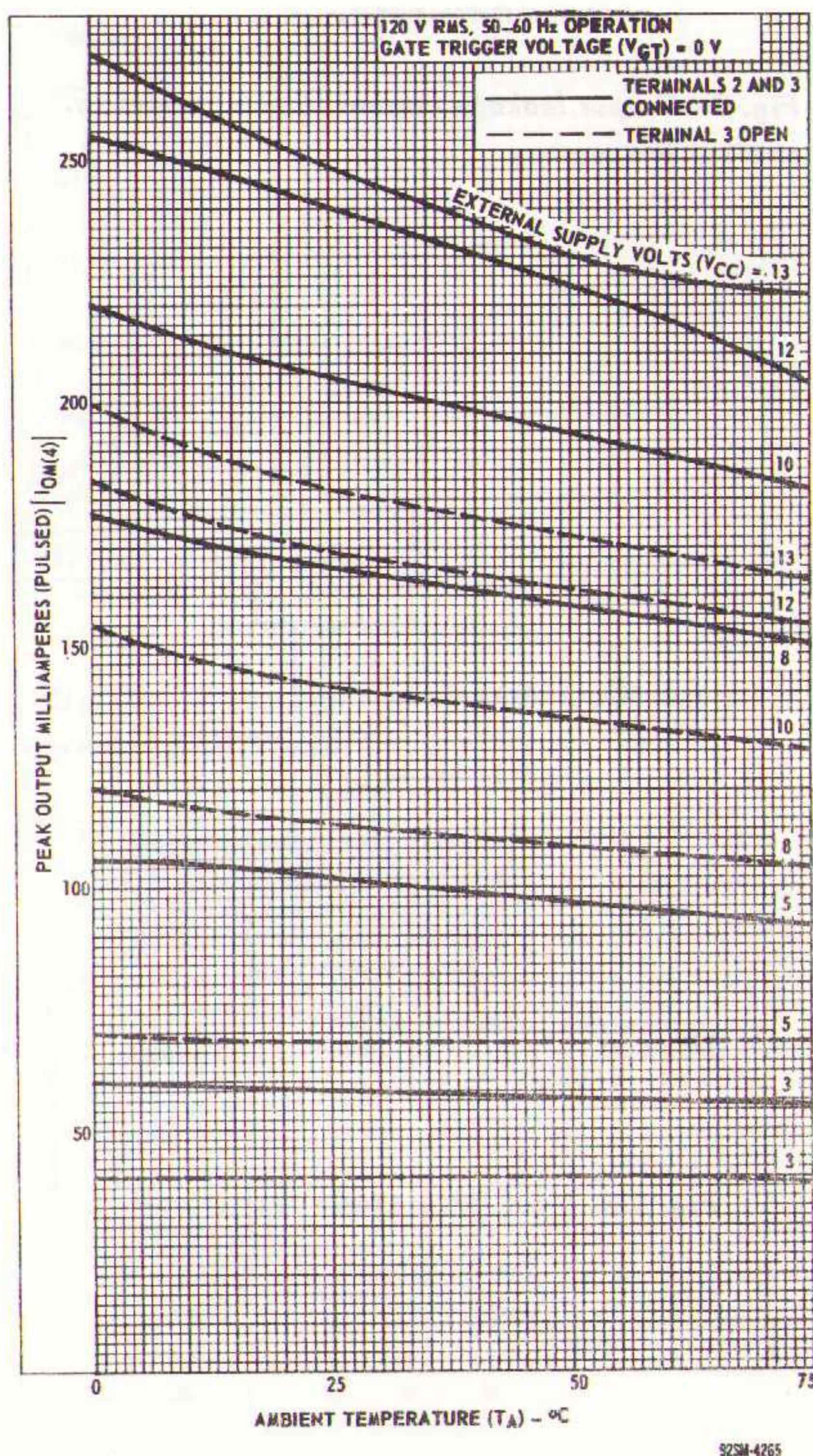


Fig. 6c - Peak output current (pulsed) with external power supply vs. ambient temperature

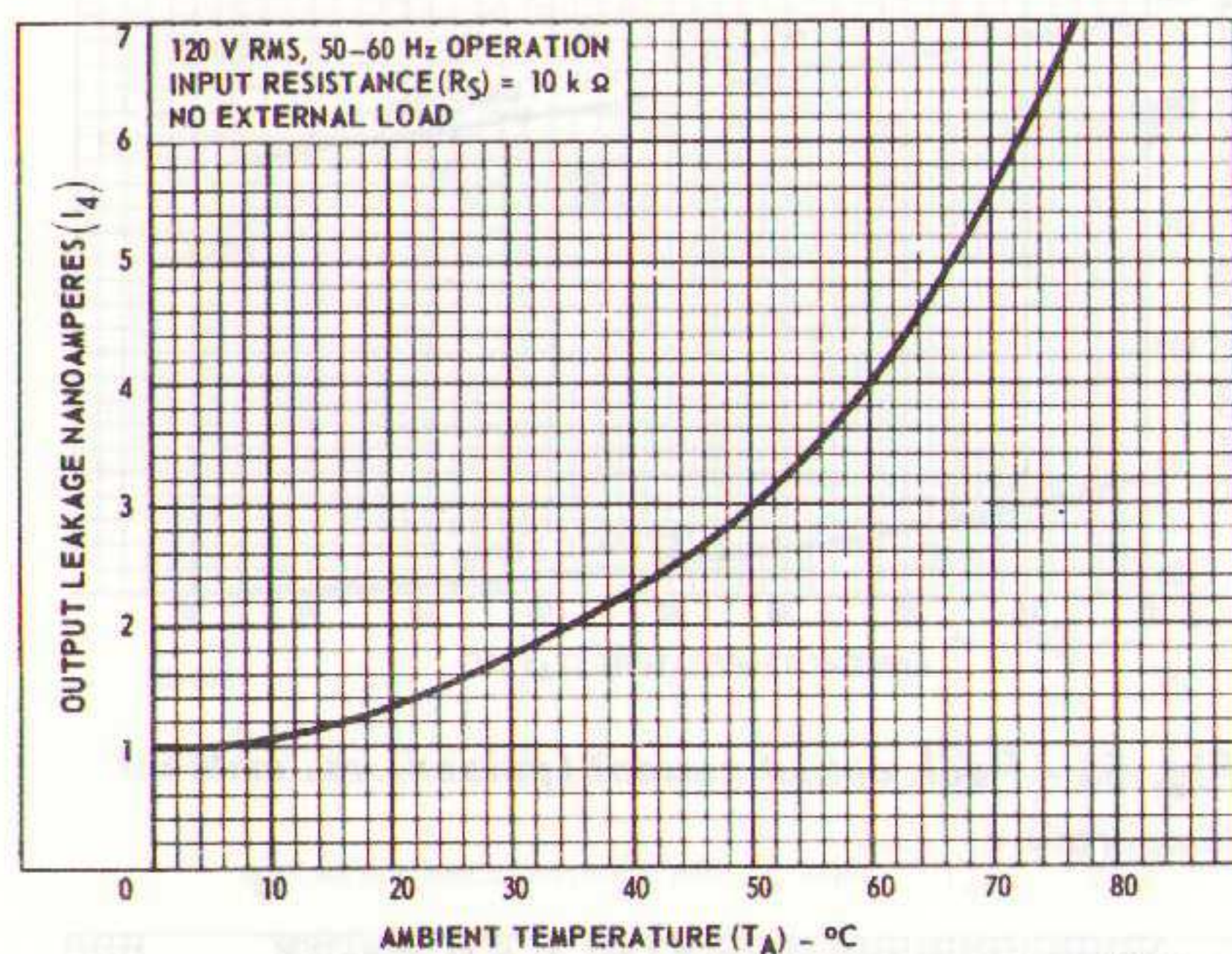


Fig. 7 - Output leakage current (inhibit mode) vs. ambient temperature

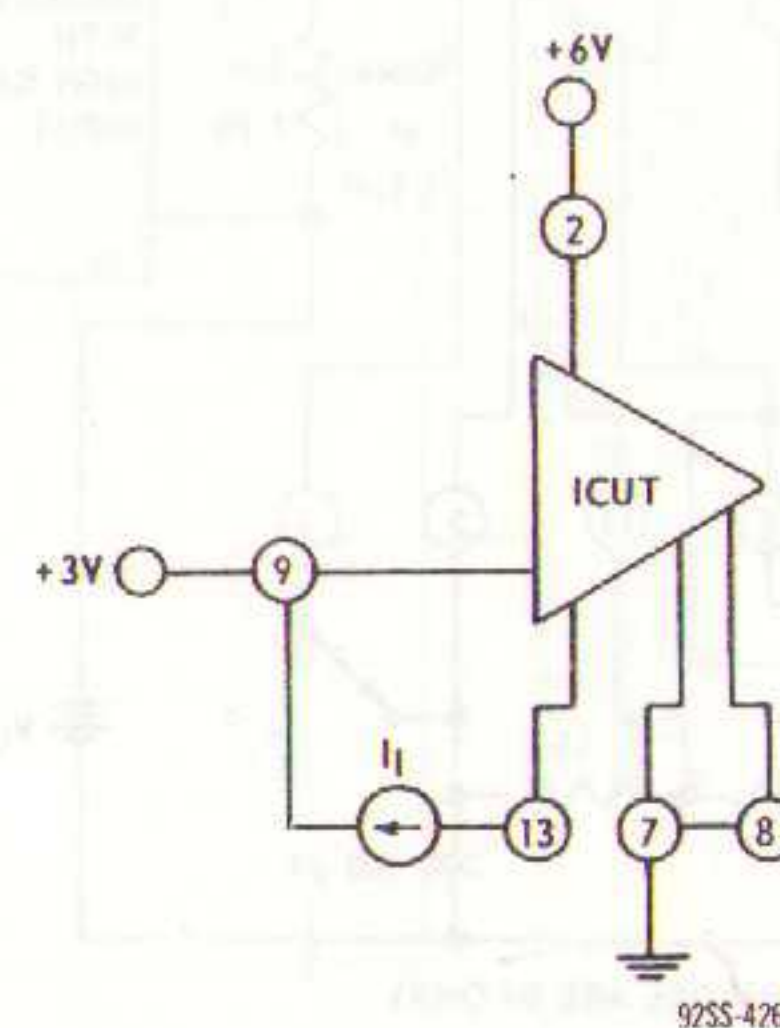


Fig. 8 - Input bias current test circuit

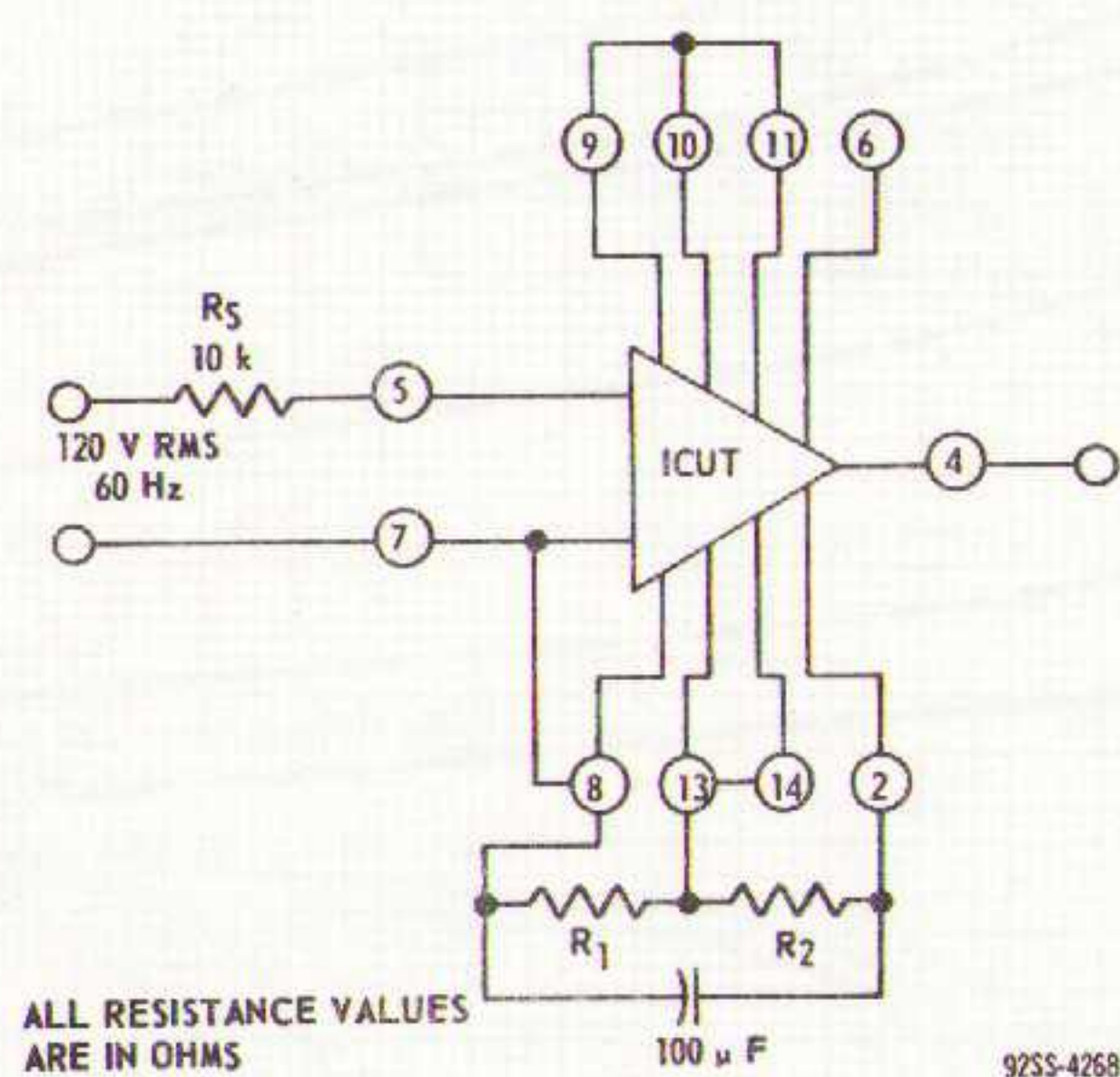


Fig. 9a - Input inhibit ratio test circuit

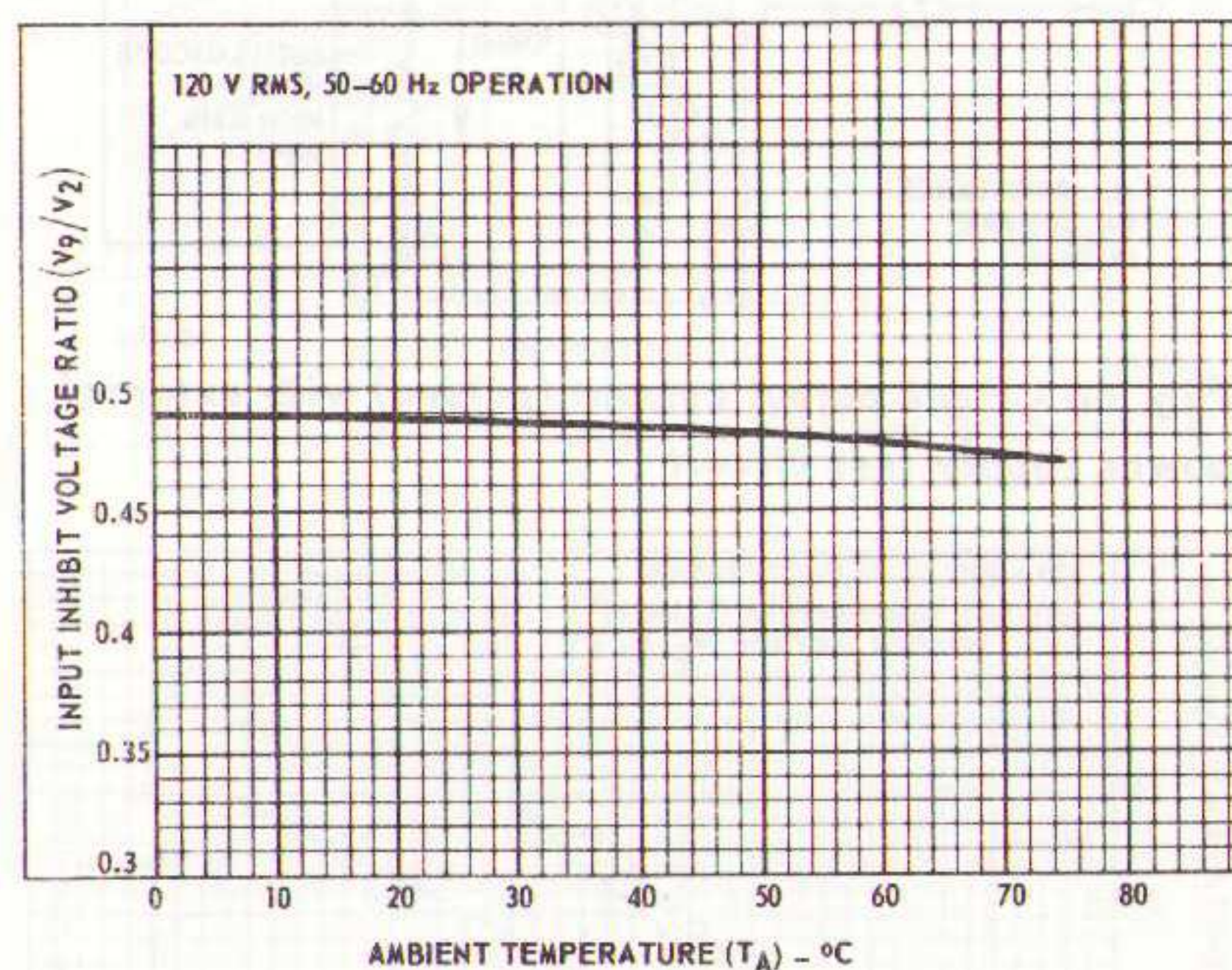
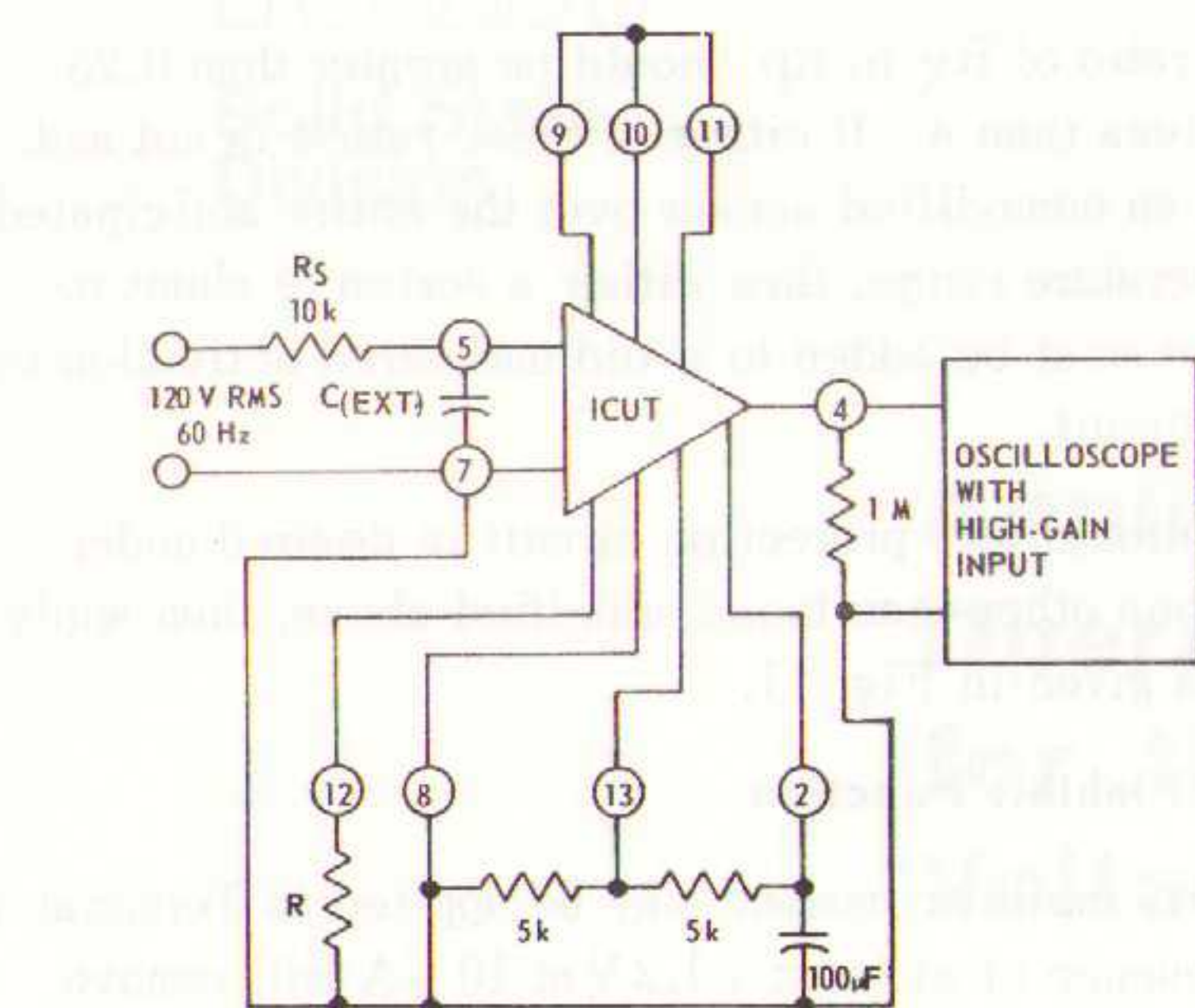


Fig. 9b.- Input inhibit voltage ratio vs. ambient temperature



ALL RESISTANCE VALUES ARE IN OHMS

Fig. 10a - Gate pulse duration test circuit

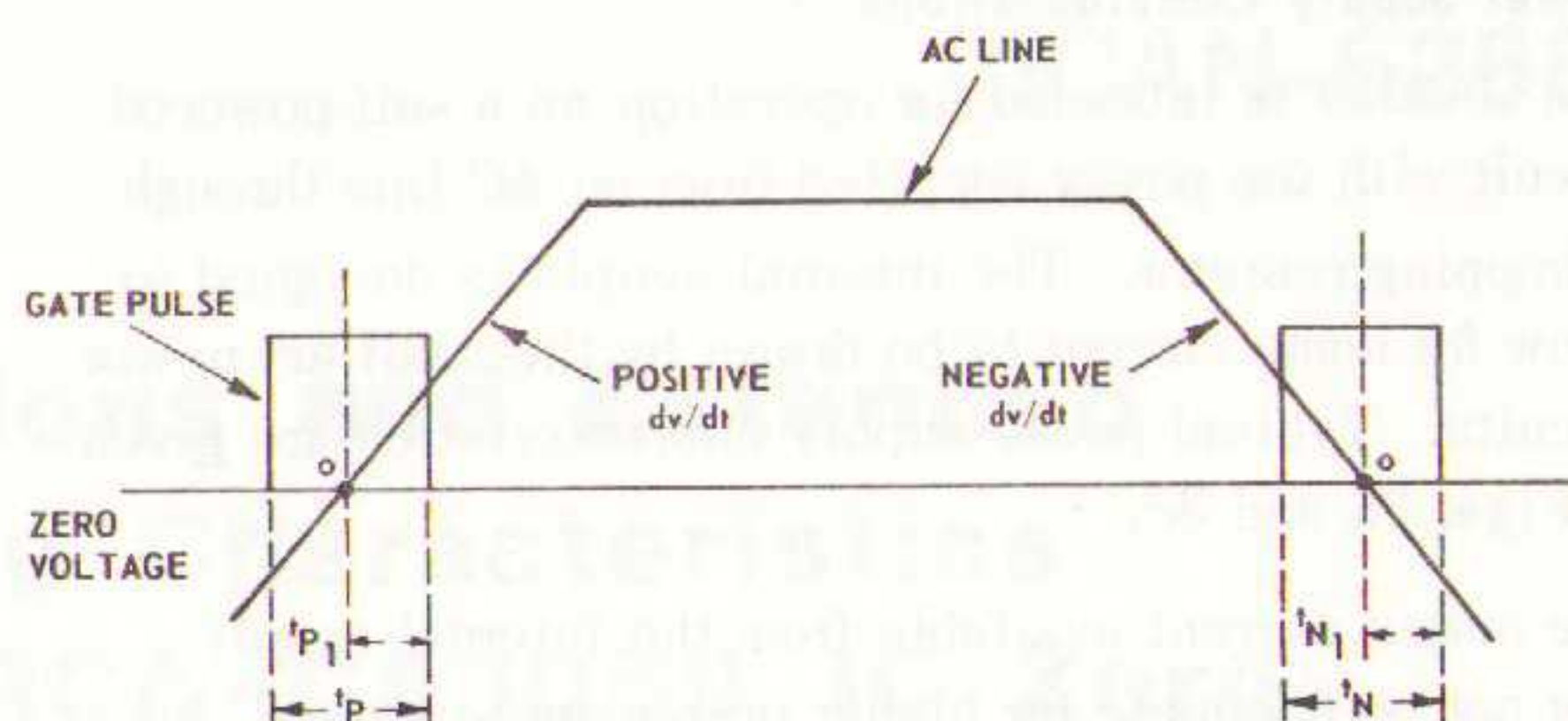


Fig. 10b - Gate pulse duration wave form

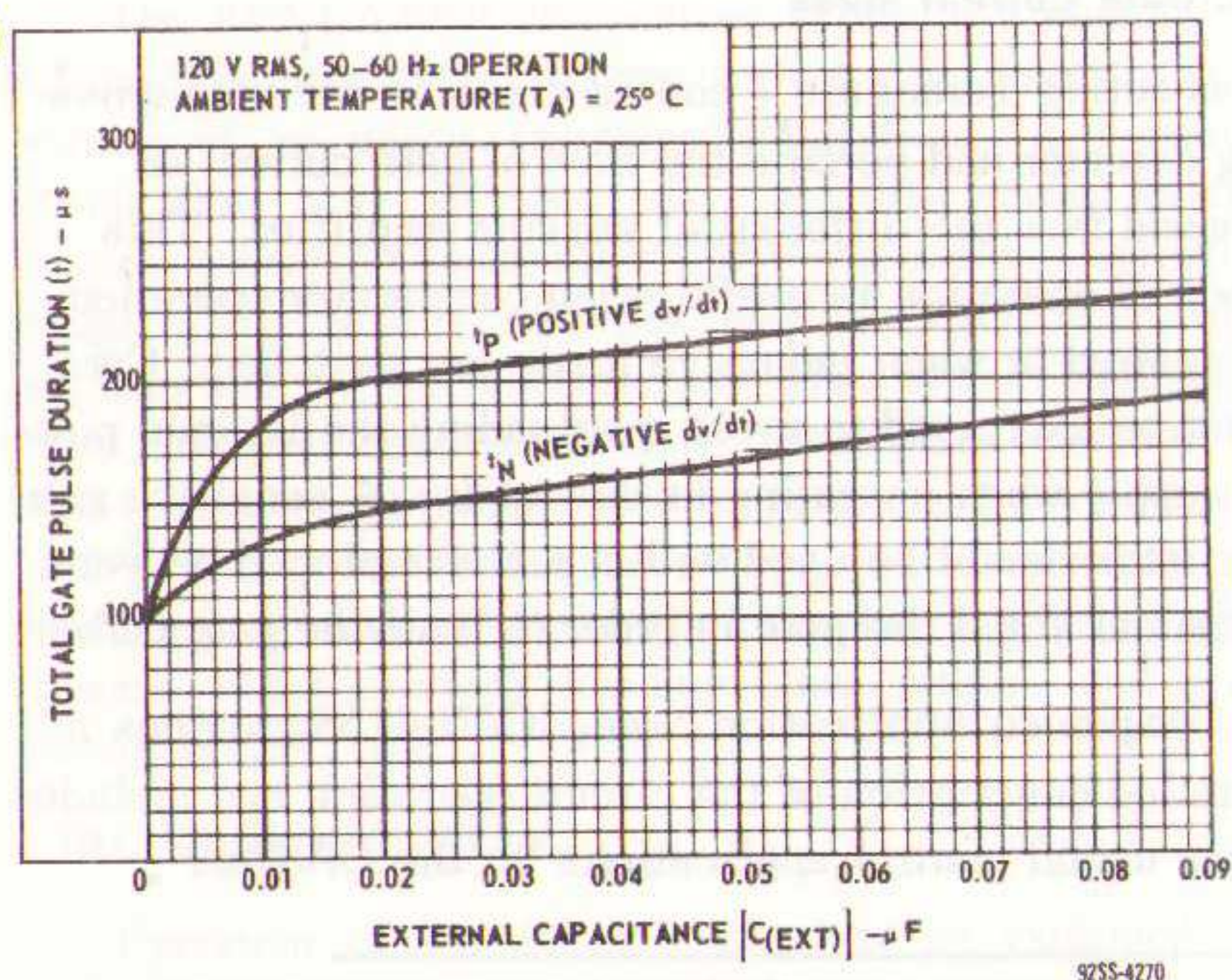


Fig. 10c - Total gate pulse duration vs. external capacitance

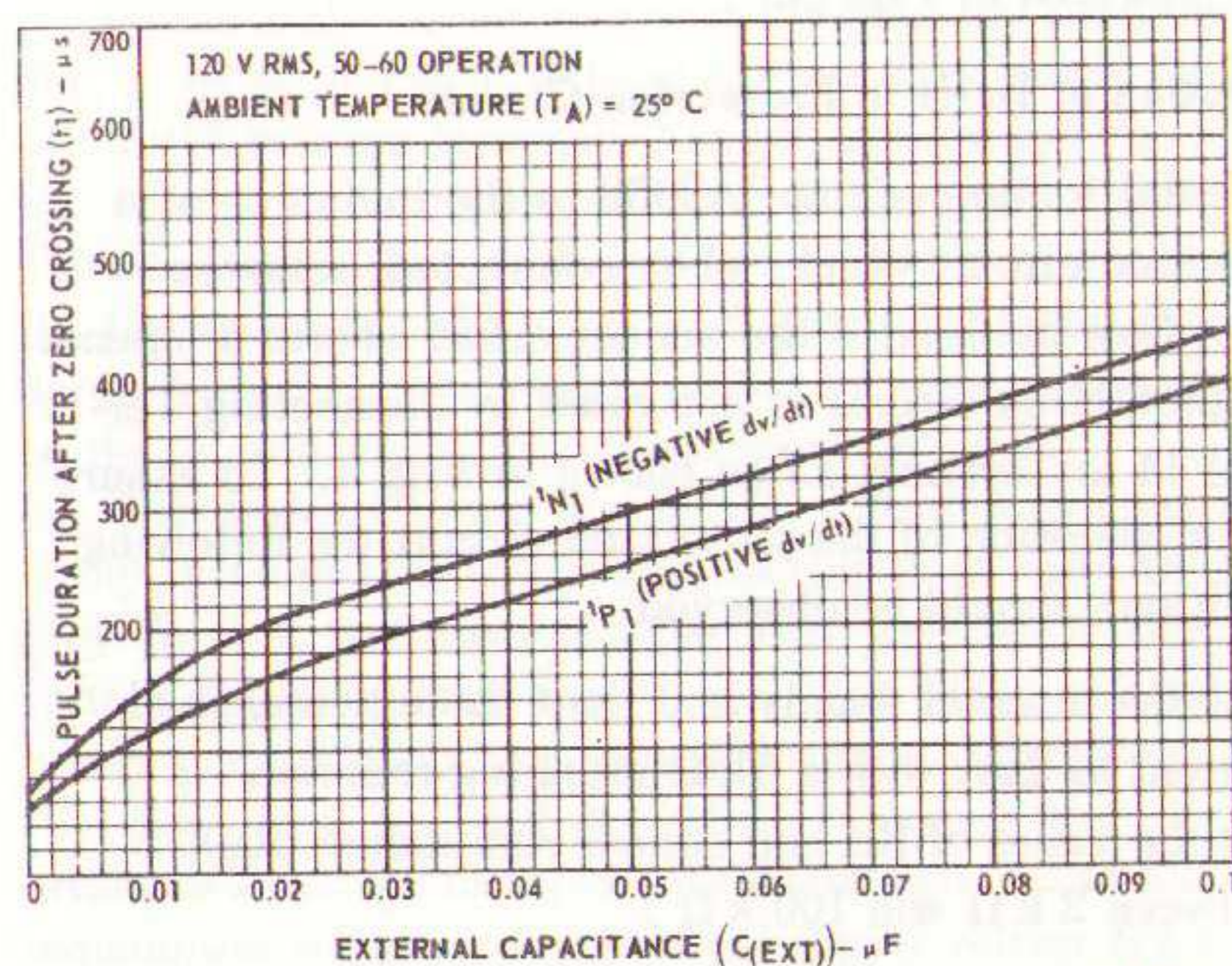


Fig. 10d - Pulse duration after zero crossing vs. external capacitance

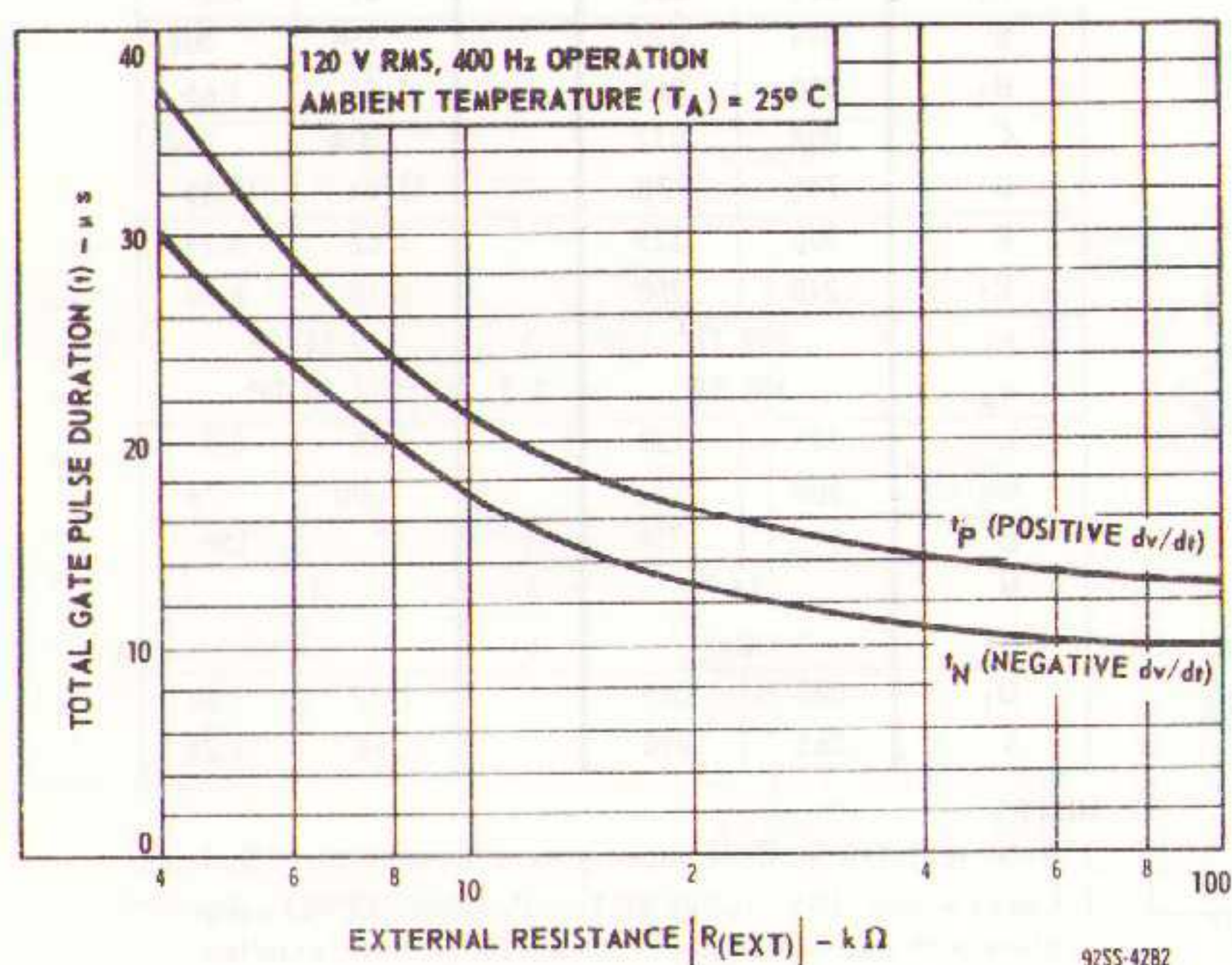


Fig. 10e - Total gate pulse duration vs. external resistance

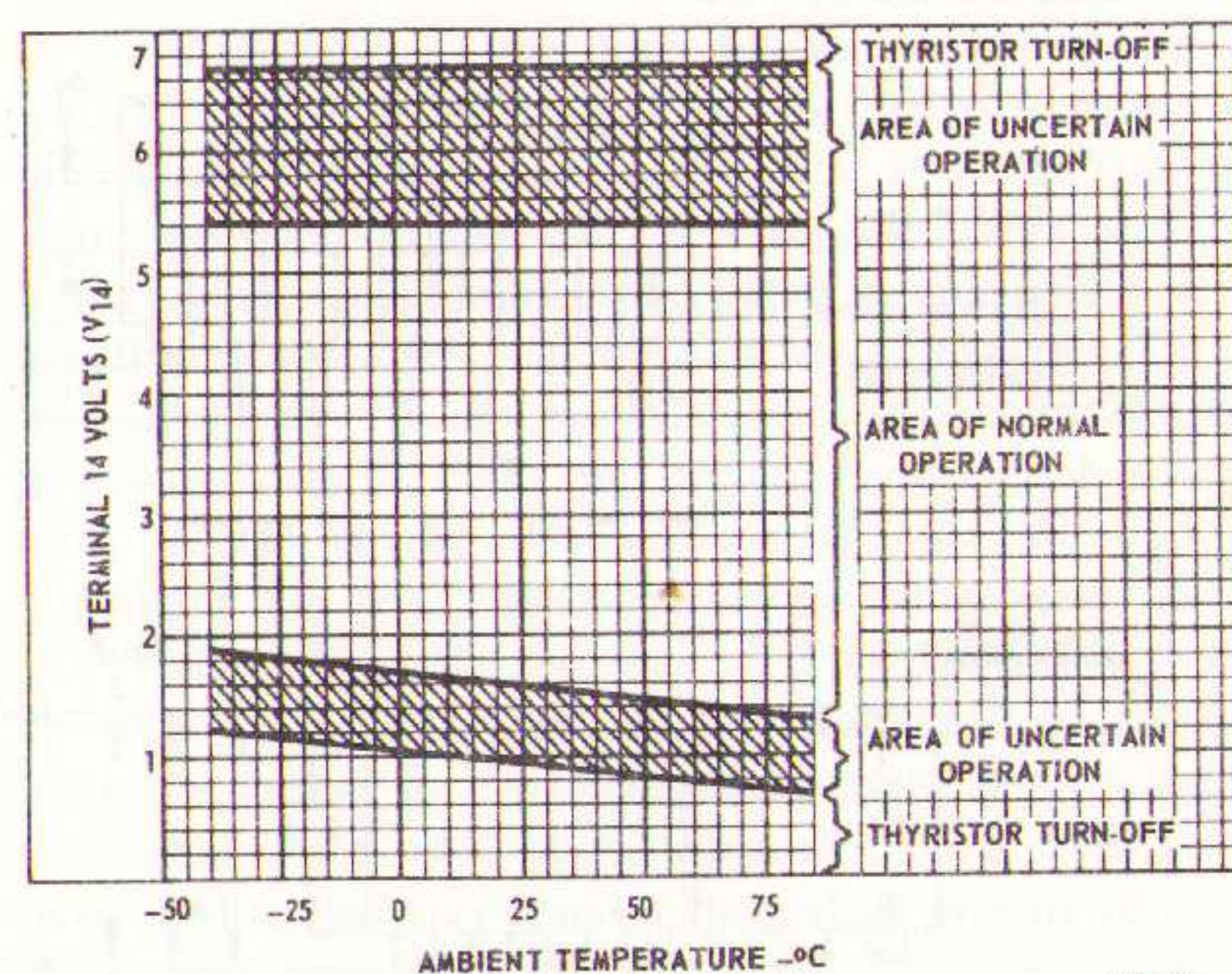


Fig. 11 - Operating regions for built-in protection circuit

OPERATING CONSIDERATIONS

Power Supply Considerations

The CA3059 is intended for operation as a self-powered circuit with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3b and 3c.

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5b for the peak output current characteristics.) When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5a.

Operation of Built-in Protection Circuit

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5k Ω dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 k Ω and 100 k Ω .

3. The ratio of R_X to R_P should be greater than 0.25 and less than 4. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 11.

External Inhibit Function

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μ A will remove drive from the thyristor. This required level is compatible with DTL or T²L logic. A logical 1 activates the inhibit function.

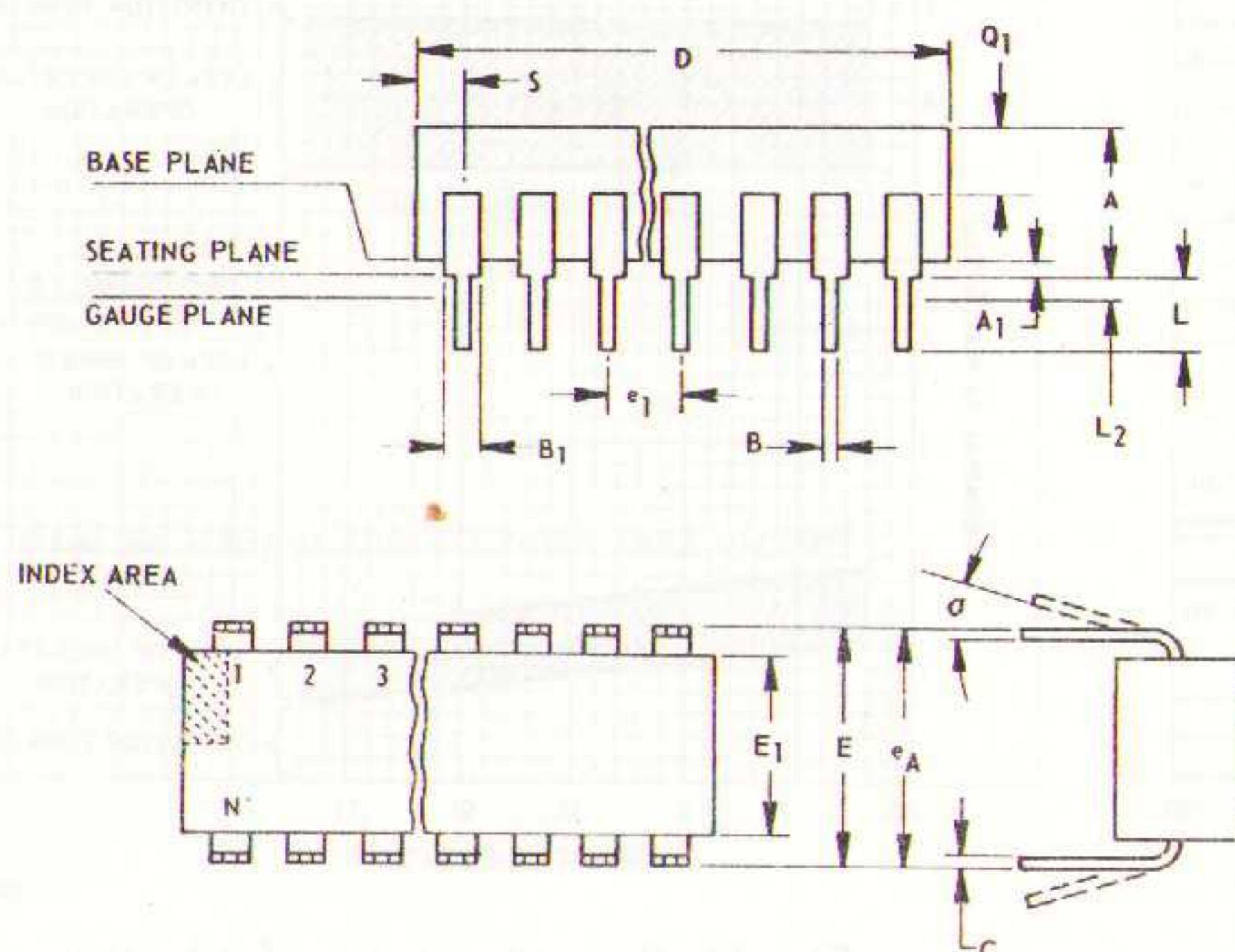
DC Gate Current Mode

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

A Companion Application Note, ICAN-4158 provides a detailed description of the circuit operation and includes many useful control applications for the CA3059.

DIMENSIONAL OUTLINE

14-Lead Dual-In-Line Plastic Package
JEDEC M0-001-AB



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN	MAX		MIN	MAX
A	.155	.200		3.94	5.08
A ₁	.020	.050		.51	1.27
B	.014	.020		.356	.508
B ₁	.050	.065		1.27	1.65
C	.008	.012		.204	.304
D	.745	.770		18.93	19.55
E	.300	.325		7.62	8.25
E ₁	.240	.260		6.10	6.60
e ₁	.100 TP		2	2.54 TP	
e _A	.300 TP		2, 3	7.62 TP	
L	.125	.150		3.18	3.81
L ₂	.000	.030		.000	.76
α	0°	15°	4	0°	15°
N	14		5	14	
N ₁	0		6	0	
Q ₁	.040	.075		1.02	1.90
S	.065	.090		1.66	2.28

NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads within .005" radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L₂ when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N₁ is the quantity of allowable missing leads.



Solid State
Division

Linear Integrated Circuits

Application Note ICAN-6268

Applications and Extended Operating Characteristics for the RCA-CA3059 IC Zero- Voltage Switch

by H. M. Kleinman and A. Sheng

The RCA-CA3059 zero-voltage switch is a monolithic silicon integrated circuit designed to control a thyristor in a variety of ac power switching applications. A previous Application Note (ICAN-4158) described several useful control systems in which the CA3059 was used as a thyristor trigger. This Note briefly describes the CA3059 circuit, explains the circuit functions and basic system configurations, and gives supplemental data for extending operation to 220-volt, 50-to-60-Hz lines and temperatures from -40°C to $+85^{\circ}\text{C}$. It also discusses additional applications including the switching of inductive loads, the provision of negative gate current, operation with low-impedance sensors, and synchronous light flashers.

CIRCUIT DESCRIPTION

Operation of the CA3059 can best be explained by reference to the functional block diagram shown in Fig. 1 and the schematic diagram shown in Fig. 2. In the following discussion, all voltages are referred to terminal 7.

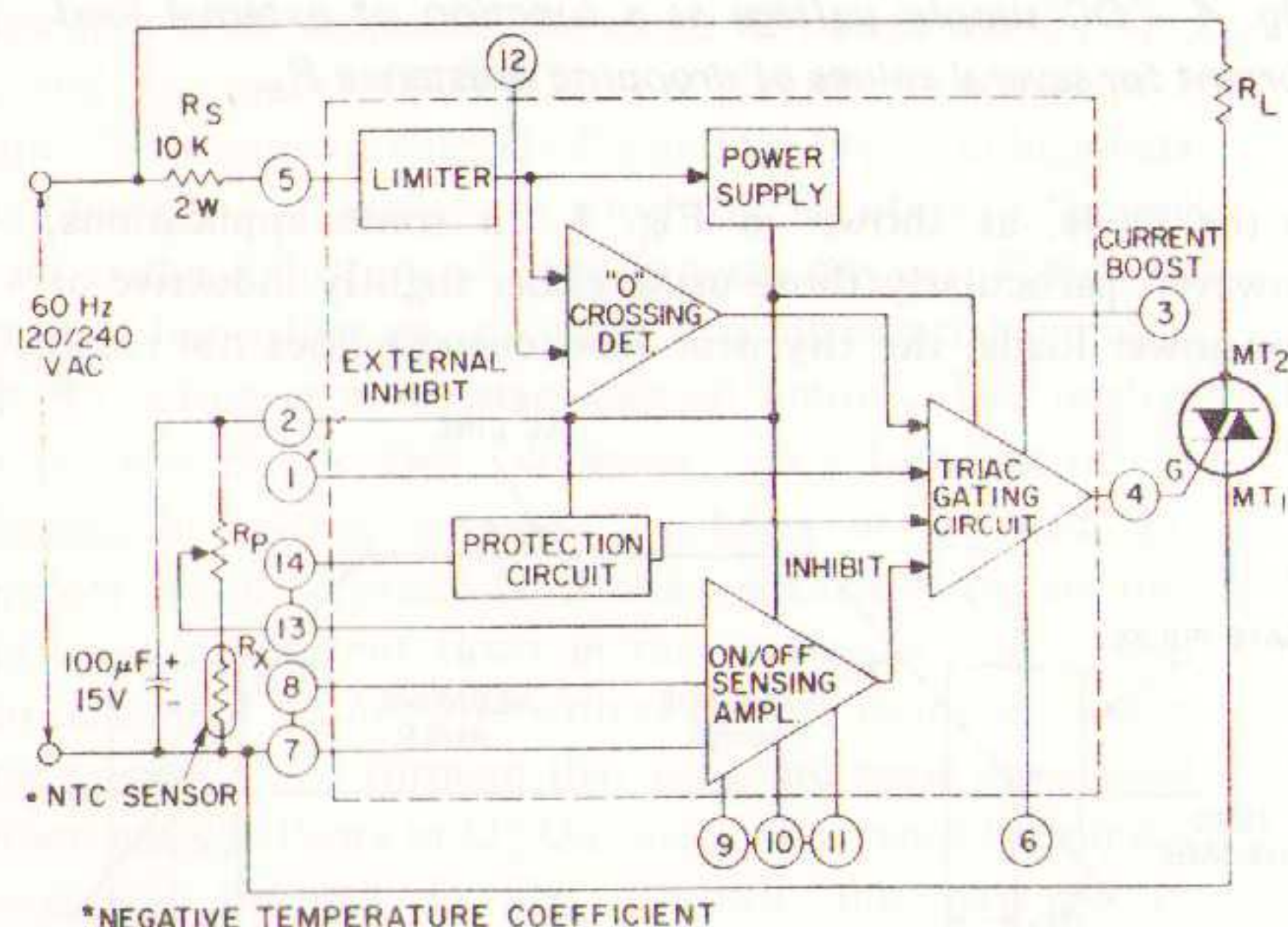


Fig. 1 - Functional block diagram of CA3059 integrated-circuit zero-voltage switch.

Power to the circuit may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 3. In the normal mode of operation, a dropping resistor R_S of 5000 to 10,000 ohms is required to limit the current in the IC. The choice of resistor is a function of the average current drawn from the power supply, either by external circuits or by the thyristor trigger circuits, as shown in Fig. 4.

The diodes D_1 and D_2 in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ± 8 volts; D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor. When an external power supply is used to increase the current capability of the IC, care must be used to avoid exceeding the 14-volt breakdown voltage rating between terminals 2 and 5. This requirement is not a problem if the supply voltage is 6 volts or less. If higher supply voltages are required, terminal 5 must be shorted to terminal 7 and the line synchronizing voltage applied to terminal 12 through a resistor of 10,000 ohms or more, as shown in Fig. 3.

The functions of the other blocks in Fig. 1 can best be understood by consideration of the normal state of a thyristor gating circuit as its ON state, in which current is being delivered to the triac gate through terminal 4. The other circuit blocks inhibit the gating circuit unless certain conditions are met. In the ON state, Q_8 and Q_9 are conducting, Q_7 is off, and Q_6 is on. Any action that turns Q_7 on removes the drive from Q_8 and allows the thyristor to turn off. Q_7 may be turned on directly by application of a minimum of +1.2 volts at 10 microamperes to the EXTERNAL INHIBIT terminal 1. (If a voltage of more than 2 volts is available, external resistance must be added to limit the current to 10 milliamperes.) Diode D_{10} isolates the base of Q_7 from other signals when an external inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher-priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Q_7 may

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Printed in USA /6-70

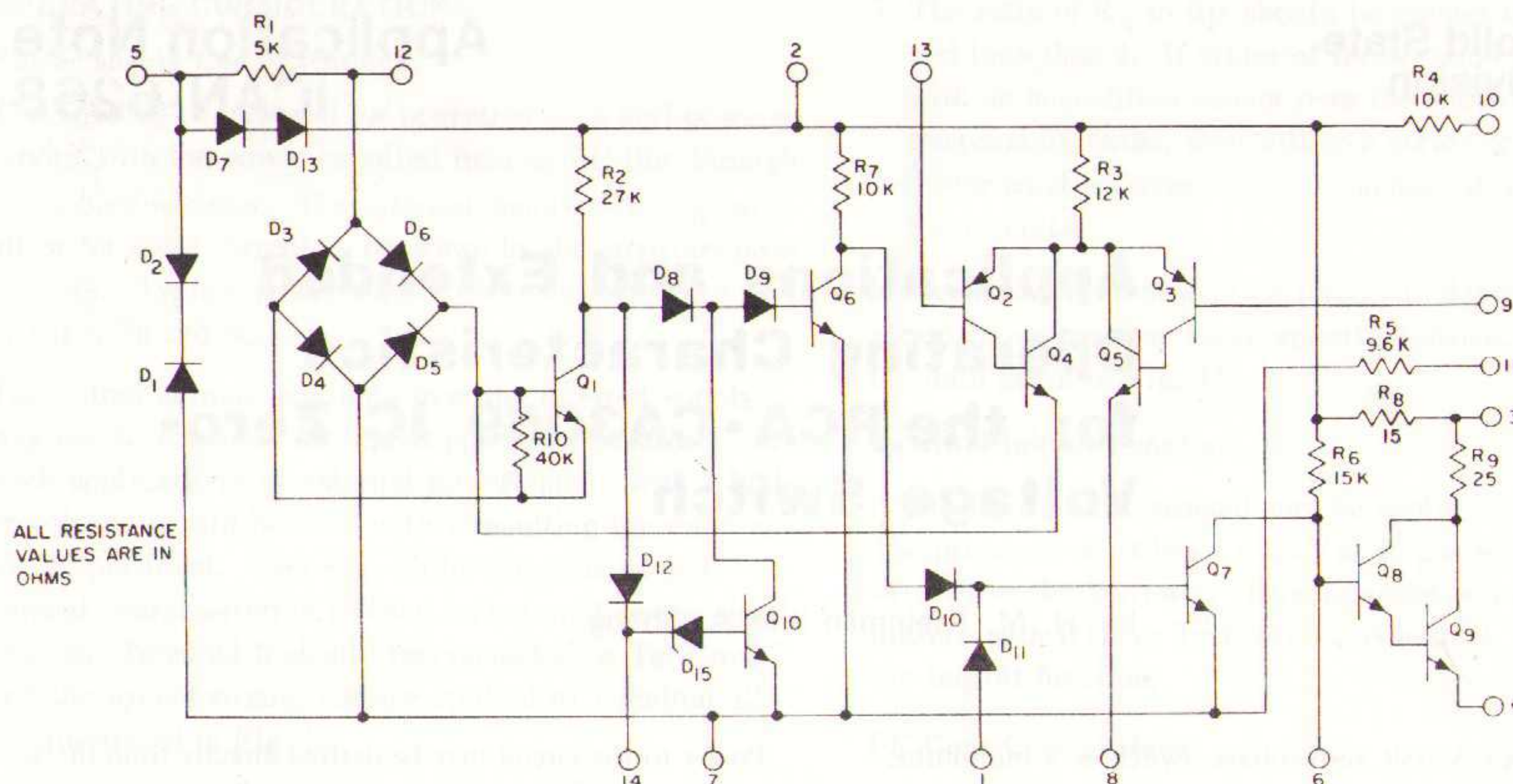


Fig. 2 - Schematic diagram of CA3059 zero-voltage switch.

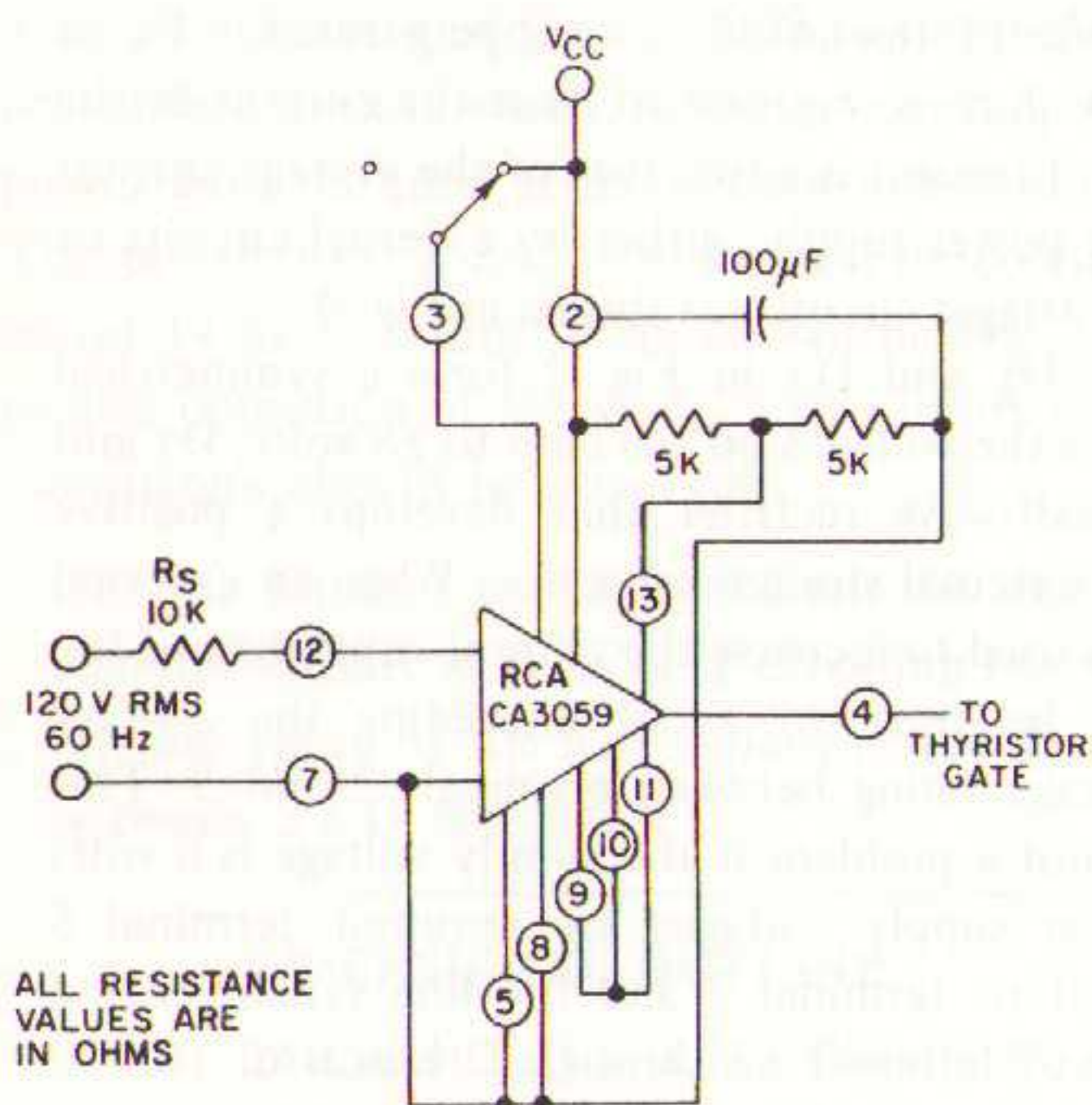


Fig. 3 - Operation of the CA3059 from an external dc power supply connected between terminals 2 and 7.

also be activated by turning off Q₆ to allow current to flow from the power supply through R₇ and D₁₀ into the base. Q₆ is normally held on by current flowing into its base through R₂, D₈, and D₉ when Q₁ is off.

Q₁ is a portion of the zero-crossing detector. When the voltage at terminal 5 is greater than +3 volts, current can flow through R₁, D₆, the base-to-emitter junction of Q₁, and D₄ to terminal 7 to turn on Q₁ and inhibit the pulse. For negative voltages with magnitudes greater than 3 volts, the current flows through D₅, the emitter-to-base junction of Q₁, D₃, and R₁, and again turns Q₁ on. Q₁ is off only when the voltage at terminal 5 is less than the threshold voltage of approximately 2 volts. When the CA3059 is connected as shown in Fig. 1, therefore, output occurs in a narrow pulse which is approximately centered about the zero-voltage time

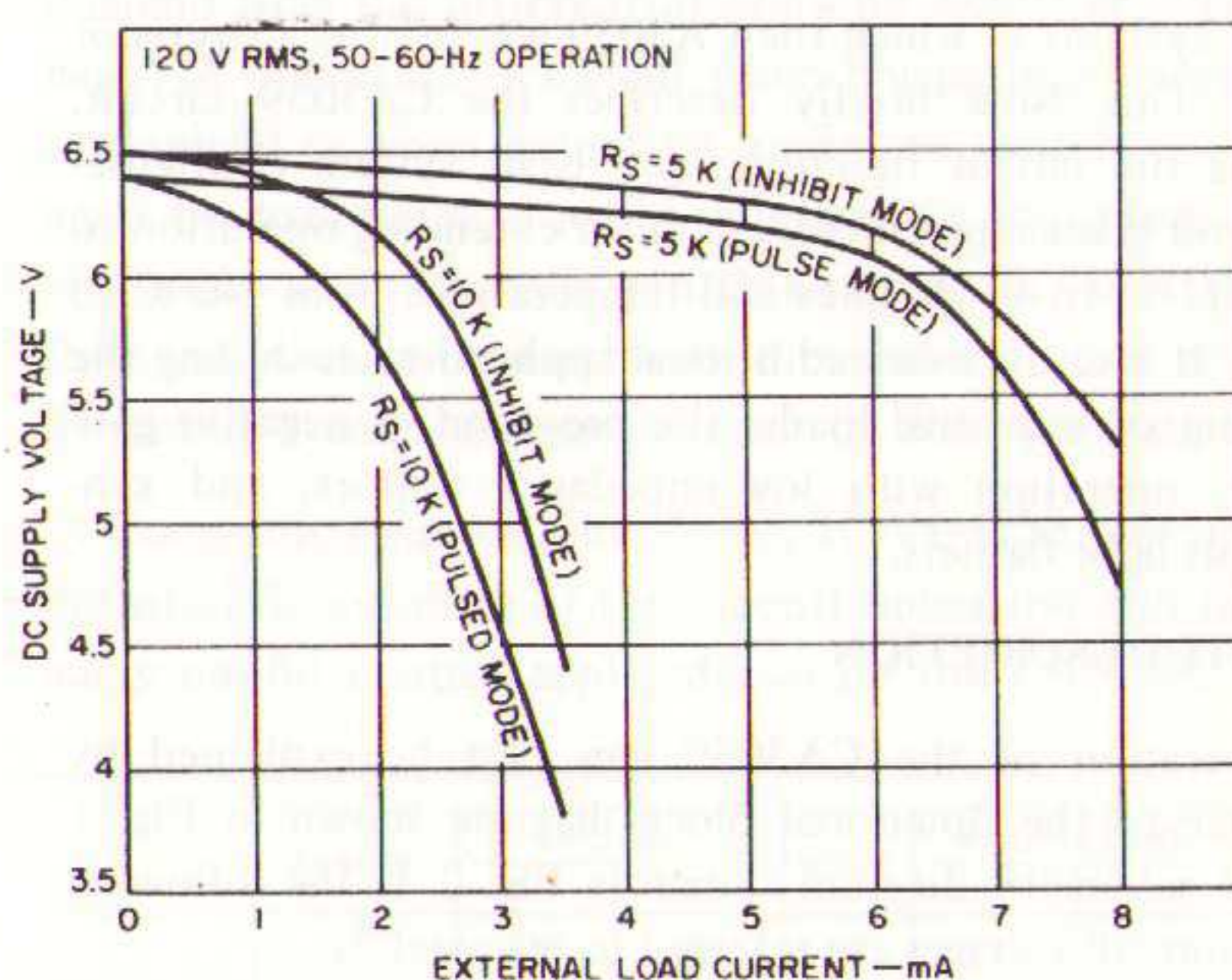


Fig. 4 - DC supply voltage as a function of external load current for several values of dropping resistance R_S .

in the cycle, as shown in Fig. 5. In some applications, however, particularly those using either slightly inductive or low-power loads, the thyristor load current does not reach

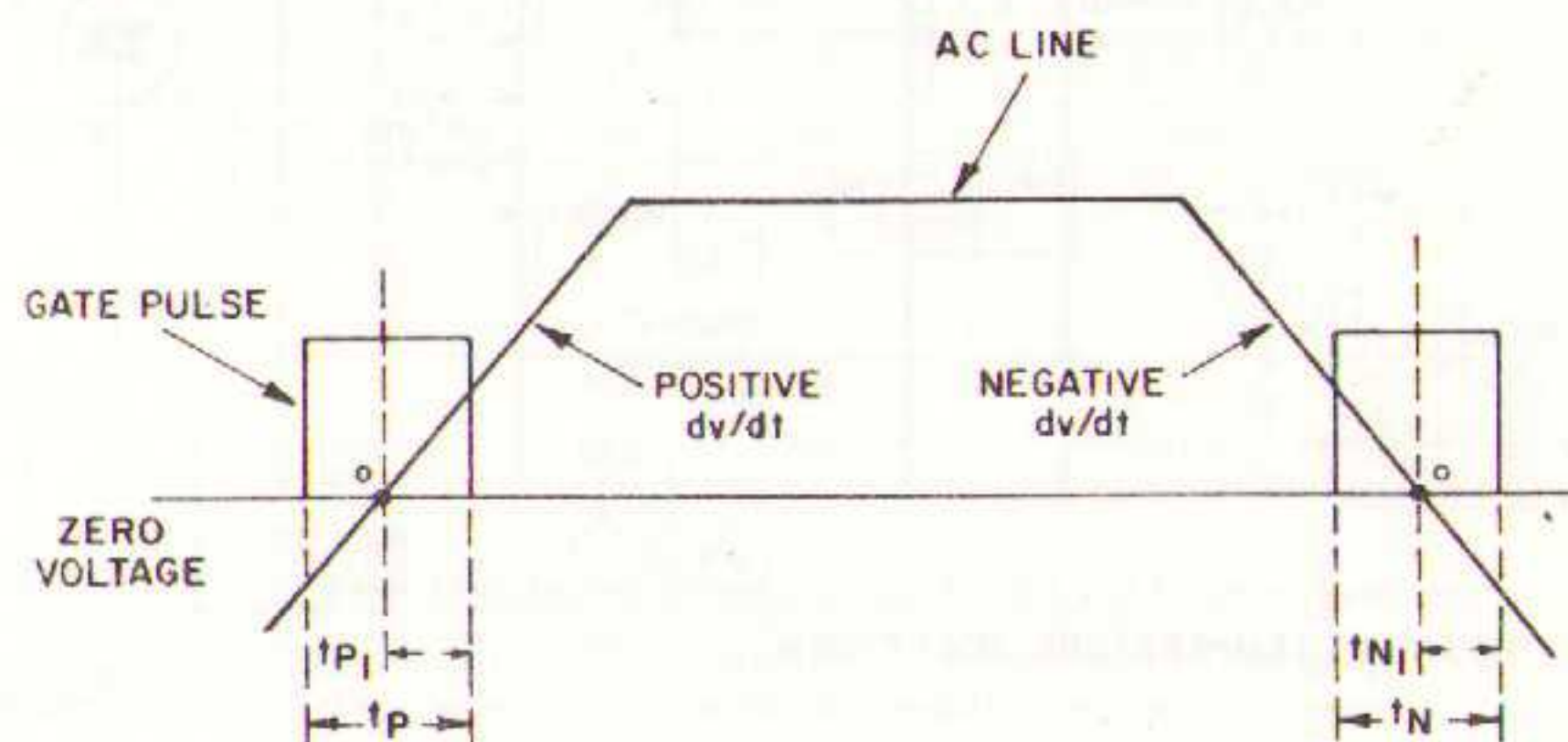


Fig. 5 - Waveform showing output-pulse duration of CA3059.

the holding current by the end of this pulse. Fig. 6 shows how an external capacitor between terminal 5 and 7 can be used to delay the pulse to accommodate such loads. The amount of pulse stretching and delay is shown in Figs. 7(a) and 7(b).

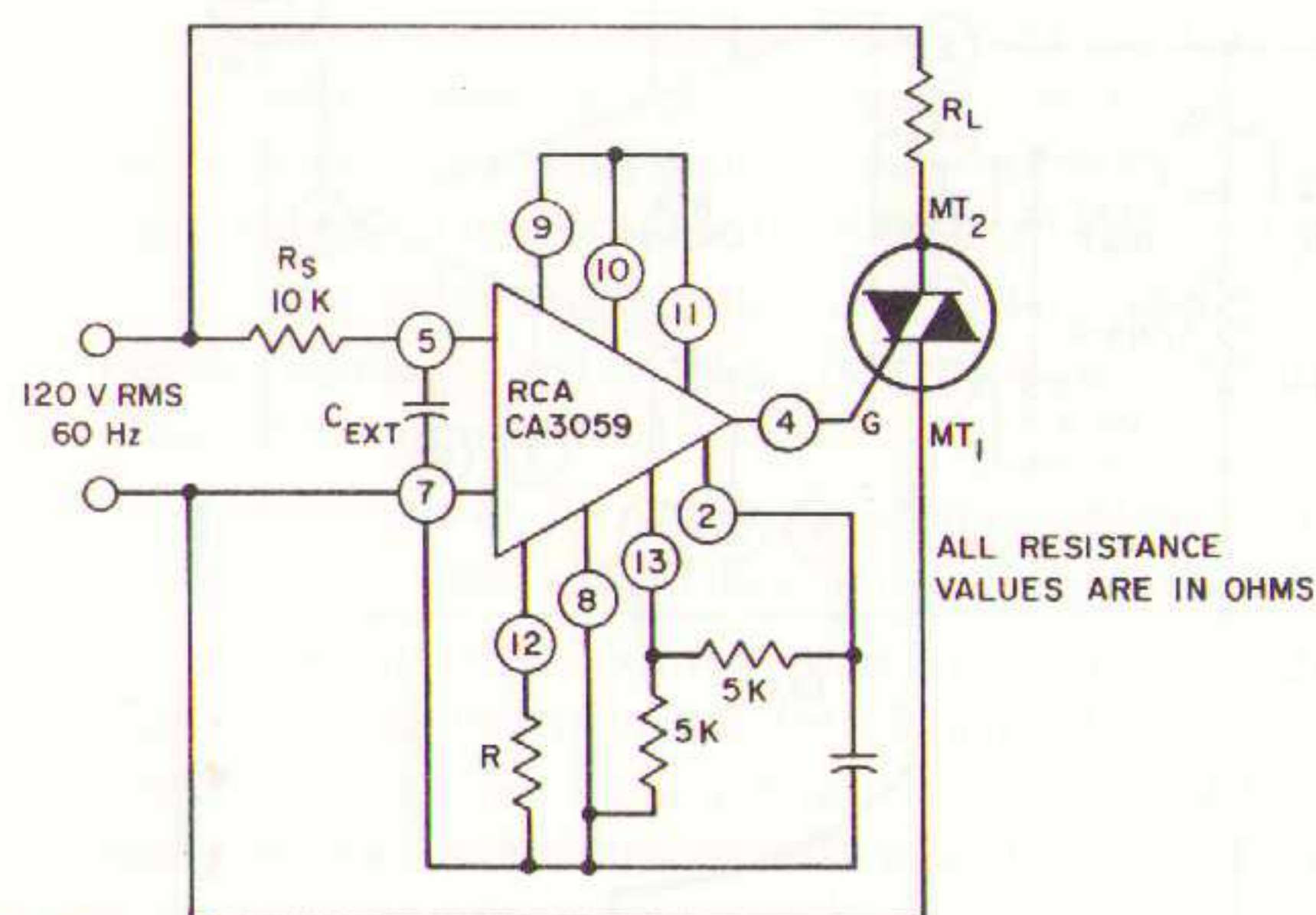


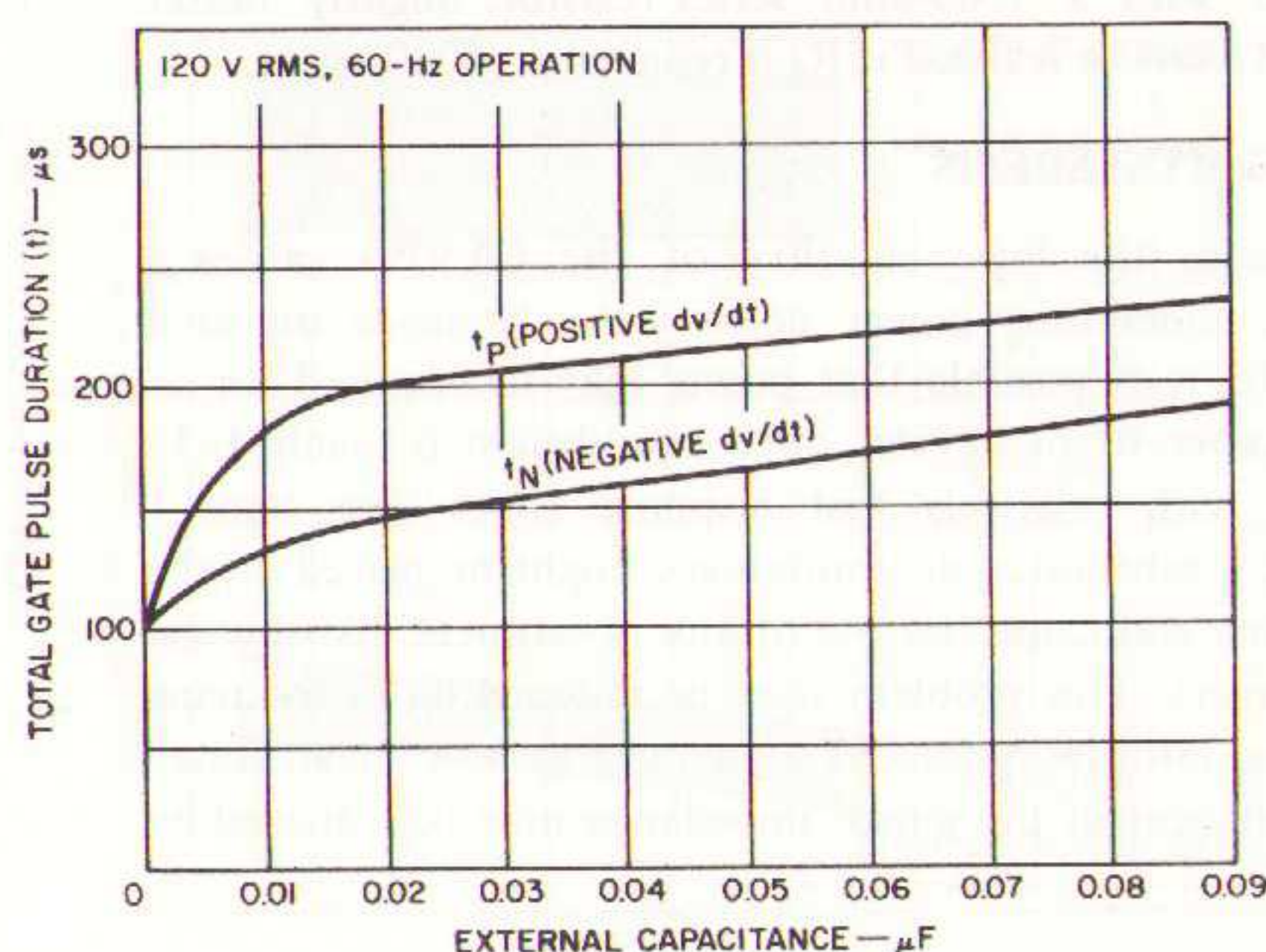
Fig. 6 - Use of a capacitor between terminals 5 and 7 to delay the output pulse of the CA3059.

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero-crossing detector. In this mode, Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be used to avoid overloading of the internal power supply in this mode. A sensitive-gate thyristor should be used and a resistor placed between terminal 4 and the gate of the thyristor to limit the current.

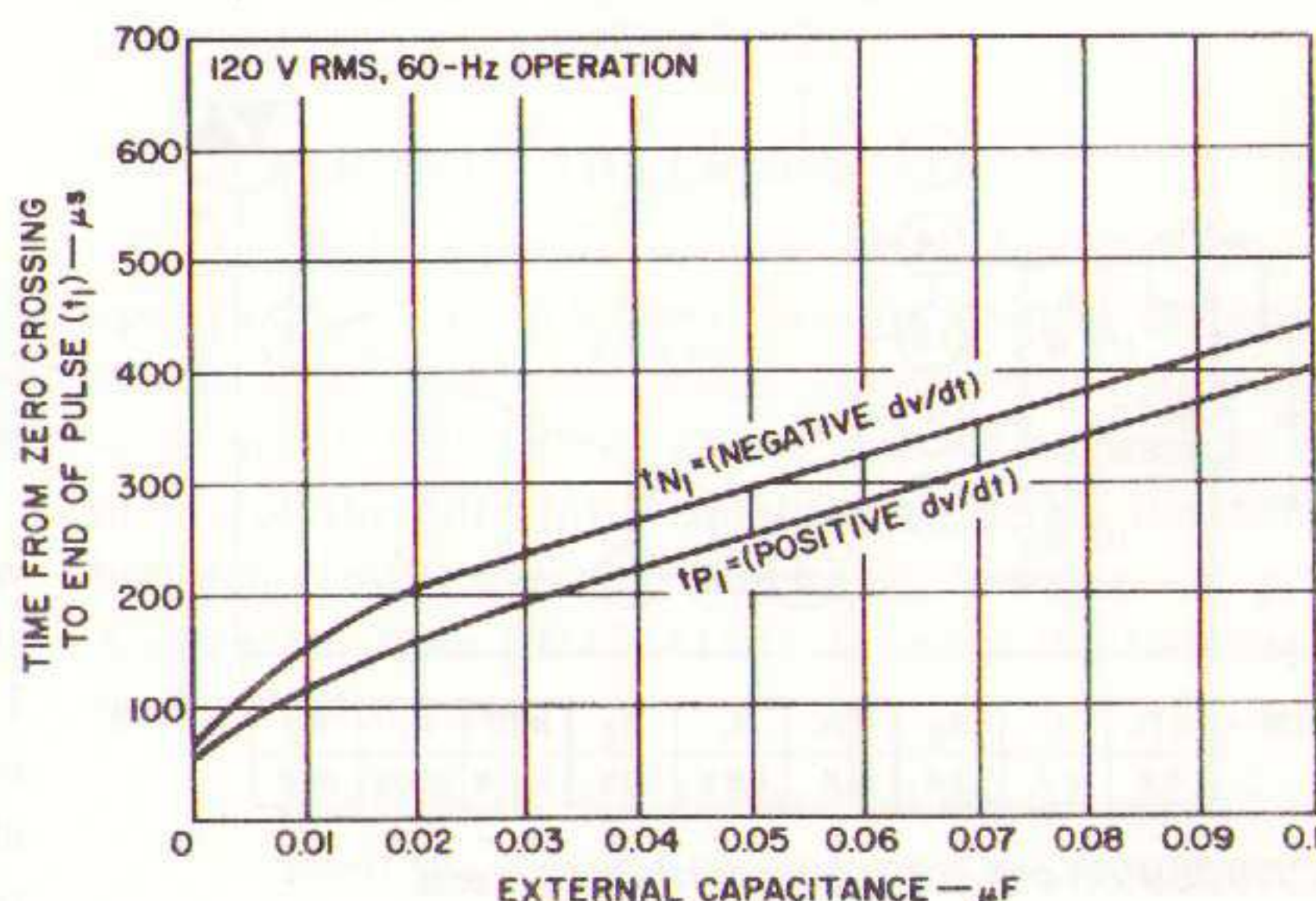
THE ON-OFF SENSING AMPLIFIER

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2 , Q_3 , Q_4 , and Q_5 makes the CA3059 a flexible power-control circuit. The transistor pairs Q_2 - Q_4 and Q_3 - Q_5 form high-beta composite p-n-p transistors in which the emitters of Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with R_3 acting as a constant-current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of Q_2 and Q_3 . Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of Q_2 - Q_4 ; when terminal 13 is negative with respect to terminal 9, most of the current flows through that path and none in terminal 8. When current flows in Q_2 - Q_4 , the path is from the supply through R_3 , through Q_2 - Q_4 , through the base-emitter junction of Q_1 , and finally through D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9 , Q_1 is on and output is inhibited.

In the circuit shown in Fig. 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, with R_p and the NTC sensor forming the other. At low temperatures, the large value of the sensor causes terminal 13 to be positive with respect to



(a)



(b)

Fig. 7 - Curves showing effect of external capacitance on (a) the total output-pulse duration, and (b) the time from zero crossing to the end of the pulse.

terminal 9 so that the thyristor fires on every half-cycle and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached and V_{13} approaches V_9 . At this point, Q_2 - Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of R_p . For cooling service, either the positions of R_p and the sensor may be reversed or terminals 9 and 13 may be interchanged.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1 megohm at balance without introduction of substantial error (i.e., greater than 5 per cent). The error may be reduced if the internal bridge elements R_4 and R_5 are not used but are

replaced with resistors which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply; the curves shown in Fig. 4 should be consulted when low-impedance sensors are used. Operation with sensors as low as 300 ohms may be obtained with a 5000-ohm series resistor. Slightly better sensitivity can be realized if R_s is reduced to 4000 ohms.

ADDING HYSTERESIS

Because the logic circuitry of the CA3059 causes a decision concerning power delivery to be made on each half-cycle, it is possible that power may be required for an odd number of half-cycles once equilibrium is reached. In systems with relatively fast response times (less than 1 second), a substantial dc component might be placed on the power line and cause heating of any isolation or distribution transformers. This problem may be reduced by introducing hysteresis into the system, as shown in Fig. 8. A "dead zone" of 10 per cent of the sensor impedance may be achieved by

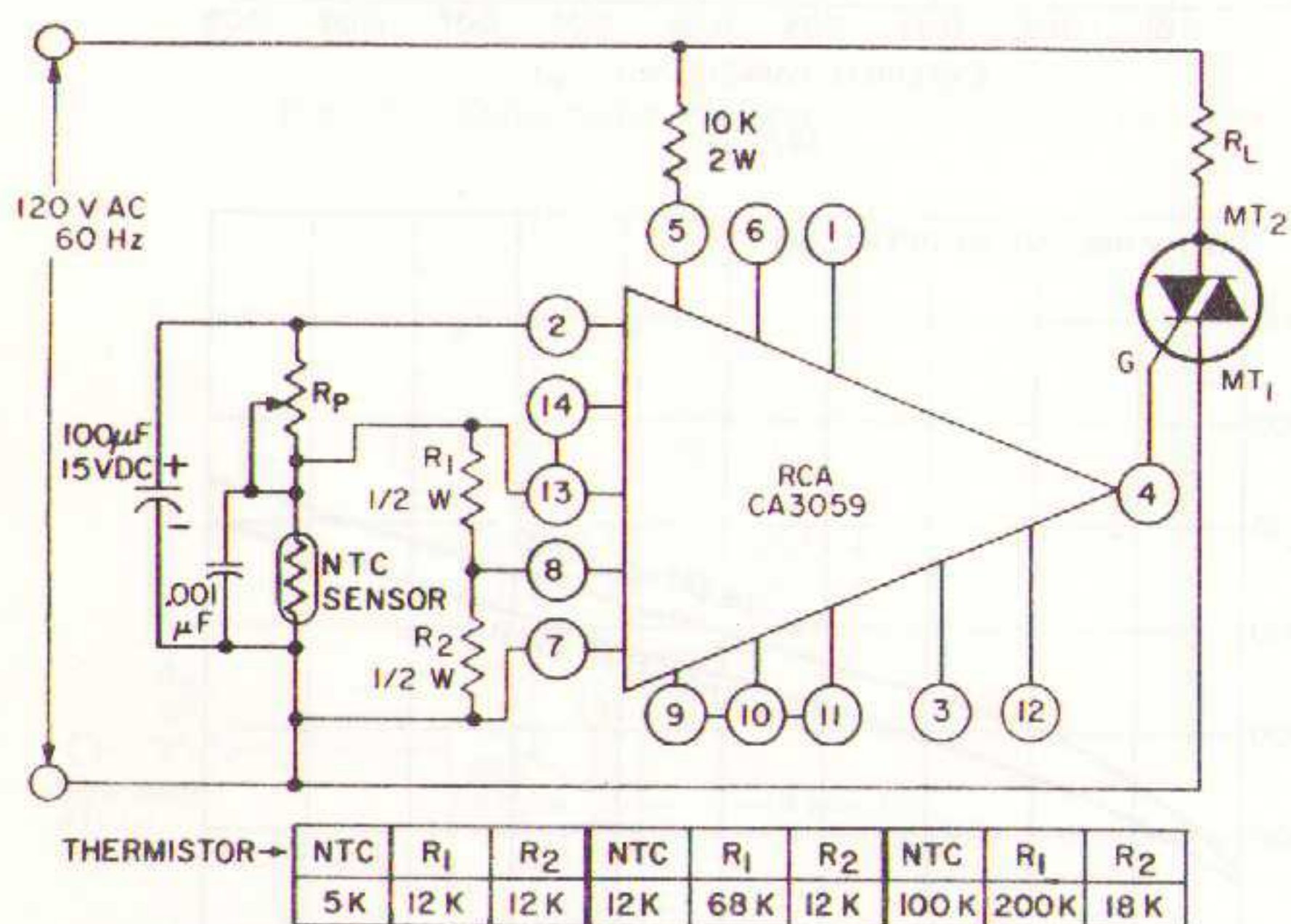


Fig. 8 - CA3059 on-off controller with hysteresis.

use of a sensor resistance R_a of 0.1 megohm, an R_1 value of 0.2 megohm, and an R_2 value of 18000 ohms. A decrease in the R_2 value reduces the effect. With a 5000-ohm sensor impedance, values of 12000 ohms for R_1 and R_2 yield a 5-per-cent dead zone. A more elaborate system (described in ICAN-4158) is required if the degree of hysteresis must be accurately controlled.

PROPORTIONAL CONTROL

The ON-OFF nature of the control shown in Fig. 1 causes some overshoot that leads to a definite steady-state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Fig. 9(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free-running multivibrator. At balance, the voltage at terminal 13 is as shown in Fig. 9 (b). When this voltage is more positive than the threshold, power is applied to the load so that the duty cycle is approximately 50 per cent. With a 0.1-megohm sensor and

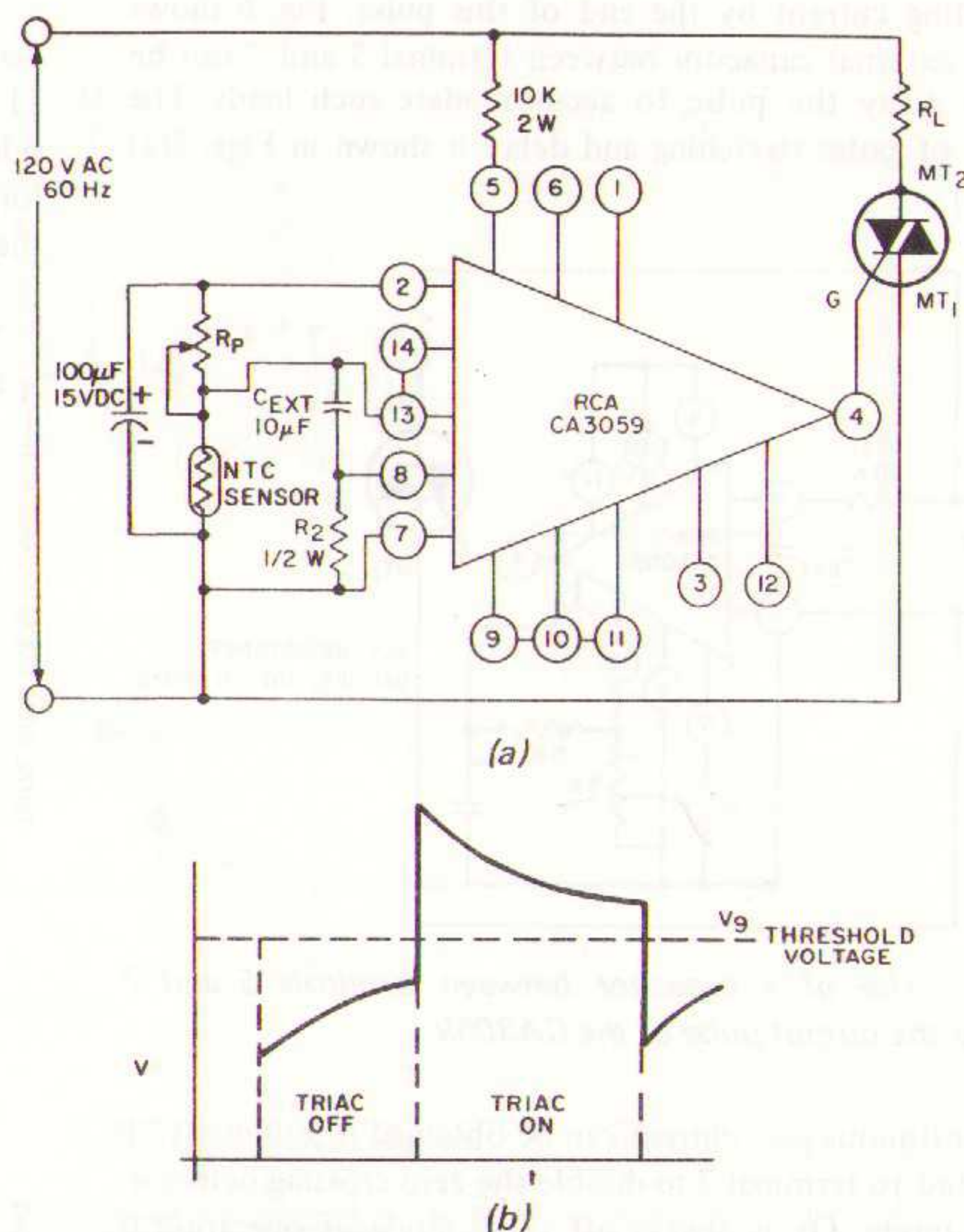


Fig. 9 - Typical heating control with proportional control: (a) schematic diagram, and (b) waveform of voltage at terminal 13.

values of $R_p = 0.1$ megohm, $R_2 = 10,000$ ohms, and $C_{ext} = 10$ microfarads, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. Changing the value of any of these elements changes the period, as shown in Fig. 10. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9 . A cooling sensor moves V_{13} in a positive direction. The triac is ON for a larger portion of the pulse cycle and increases the average power to the load.

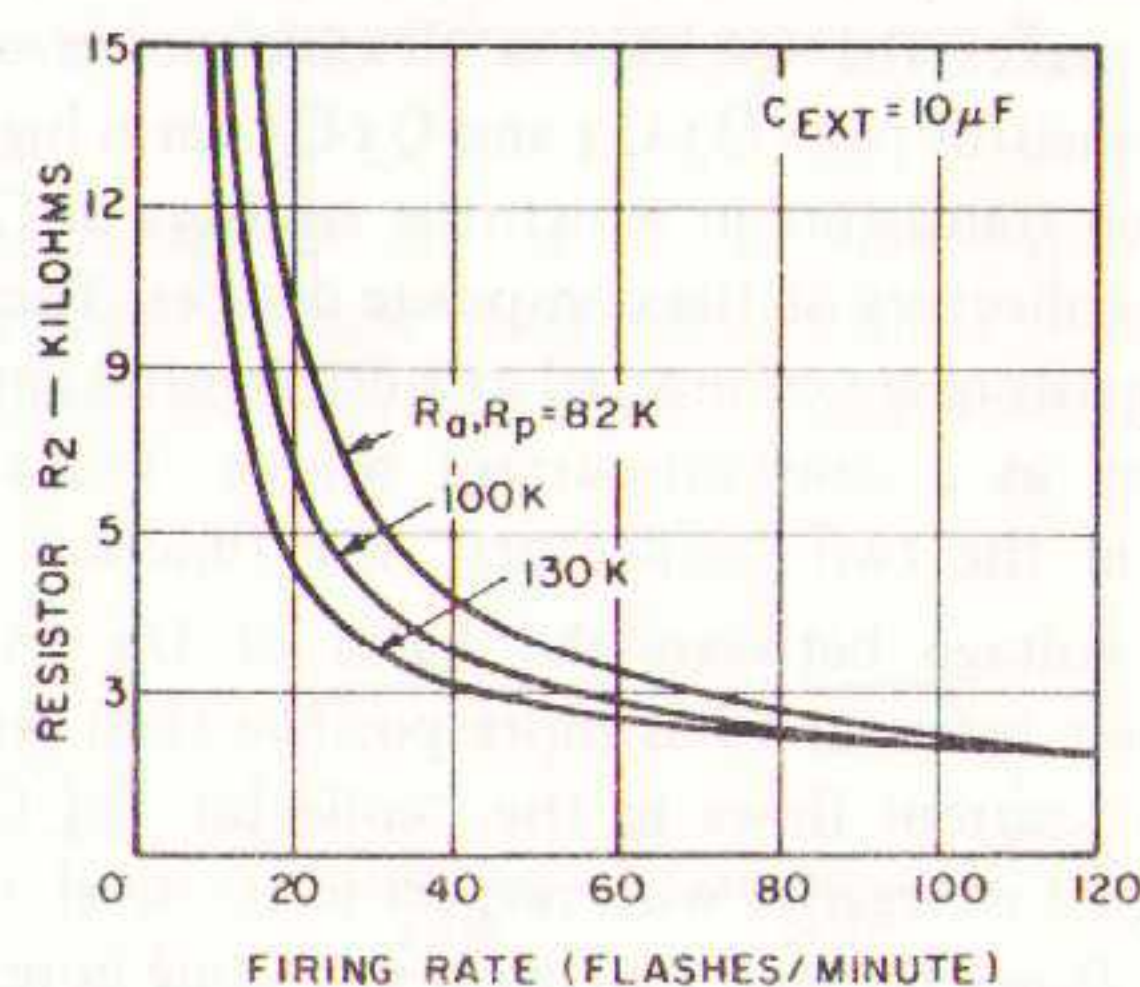


Fig. 10 - Effect of variations in time-constant elements on period.

As in the case of the hysteresis circuitry described, some special applications may require more sophisticated systems

to achieve either very precise regions of control or very long periods (see ICAN-4158).

FAIL-SAFE OPERATION

A special feature of the CA3059 is the inclusion of a fail-safe circuit which removes power from the load if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, fail-safe operation is guaranteed under the following conditions:

1. The circuit configuration of Fig. 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.
2. The value of R_p and of the sensor resistance must be between 2000 ohms and 0.1 megohm.
3. The ratio of sensor resistance and R_p must be greater than 0.25 and less than 4.0 for all normal conditions (if either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit).

Fail-safe operation may be applied to other systems when operation of the circuit is understood. The fail-safe circuit consists of D₁₂, D₁₅, and Q₁₀. D₁₂ activates the fail-safe circuit if the sensor shown in Fig. 1 shorts or drops too low in value, as follows: Q₆ is on during an output pulse so that the junction of D₈ and D₁₂ is 3 diode drops (approximately 2 volts) above terminal 7. As long as V₁₄ is more positive or only 0.15 volt negative with respect to that point, D₁₂ does not conduct and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of D₈ can have a potential of only 1.6 to 1.7 volts, and current does not flow through D₈, D₉, and Q₆; the thyristor then turns off. The actual threshold is approximately 1.2 volts at room temperature, but decreases 4 millivolts per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6 volts, the zener diode D₁₅ breaks down and turns on Q₁₀, which then turns off Q₆ and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown of D₁₅, activation of the fail-safe circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 11 shows a guide for the proper operation of the fail-safe circuit when an external supply is used.

SUPPLEMENTAL CHARACTERISTICS DATA

The characteristics curves shown in Fig. 12 are similar to curves shown in the published data for the CA3059 (RCA File No. 397, dated 10/69), but have been extended to cover the entire operating range from -40°C to +85°C. Fig. 13 presents data required for operation of the CA3059 from the 220-volt, 50-Hz lines which are common in Europe and from the 220-to-240-volt, 60-Hz lines which are commonly used for high-power applications in the United States. Although the CA3059 may be operated from any line voltage or frequency, the characteristics of the output pulse change for

different line voltages and frequencies. Figs. 13(a) and (b) show relative pulse width and location of the zero-voltage crossing when a 10,000-ohm series dropping resistor is used. Figs. 13(c) and (d) show the same information for an increased resistor value of 20,000 ohms.

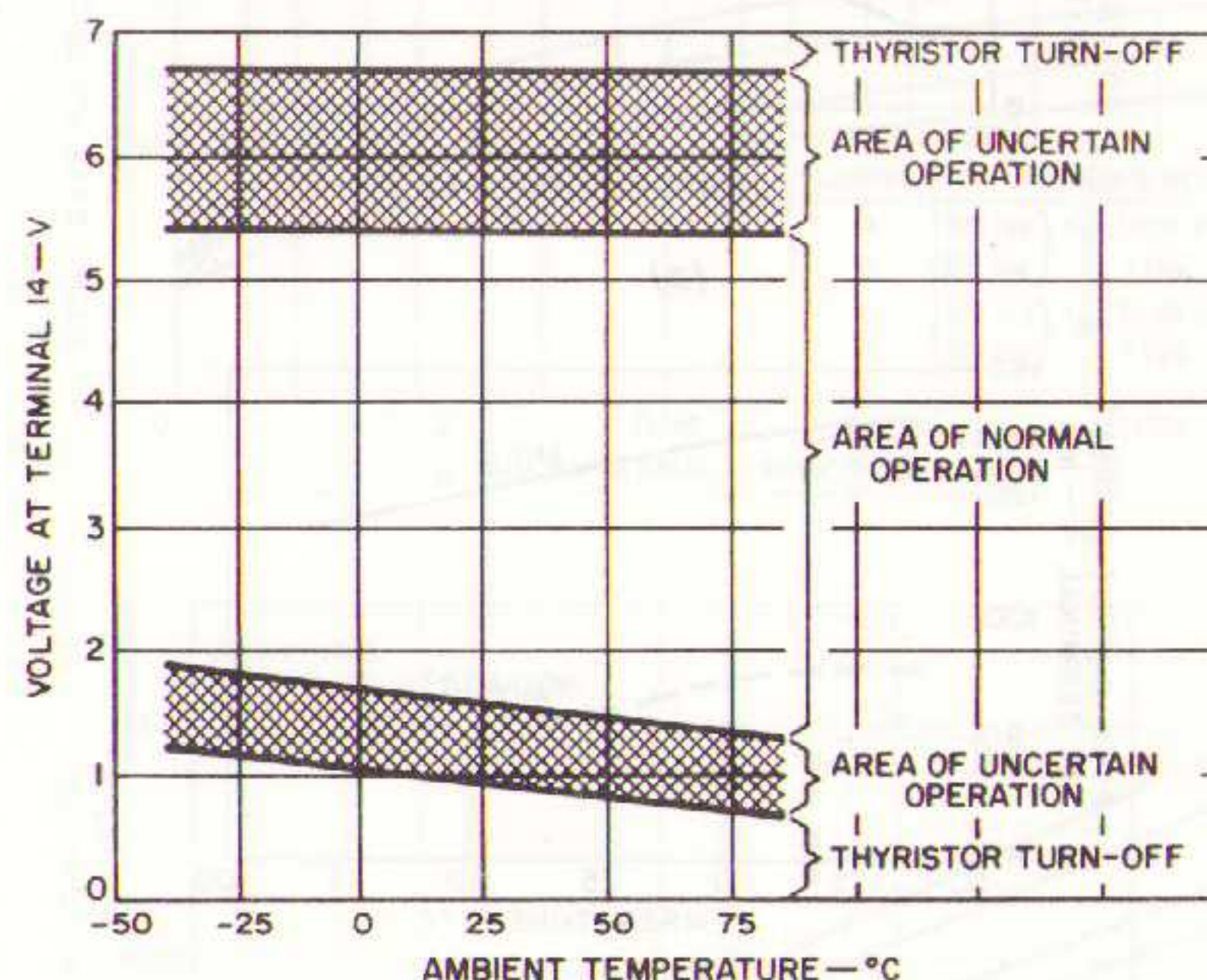


Fig. 11 - Operating regions for built-in protection circuits.

APPLICATIONS OF THE CA3059

The early sections of this Note described the basic operation of the CA3059 in heating control systems. The circuit is adaptable to many other control functions by variation of the type of sensor used or by the use of the inputs of the differential amplifier to detect the difference between two externally developed voltages. A previous Application Note (ICAN-4158) describes the following useful CA3059 systems:

- 1) a controller with an external fail-safe circuit for use when the sensor does not meet the requirements for use of the internal circuit,
- 2) a controller with provisions for accurate setting of hysteresis,
- 3) a proportional control system with an external ramp generator,
- 4) a dual-output, over-under temperature controller,
- 5) a heat staging controller,
- 6) a circuit which eliminates half-cycling,
- 7) a circuit with an isolated sensor,
- 8) a power one-shot control,
- 9) a synchronously switched traffic flasher,
- 10) transient-free switch controllers.

Although most of these circuits illustrate a heating control circuit, they are all adaptable to other control functions by change of the control logic or sensor.

SWITCHING INDUCTIVE LOADS

For proper driving of a thyristor in full-cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal

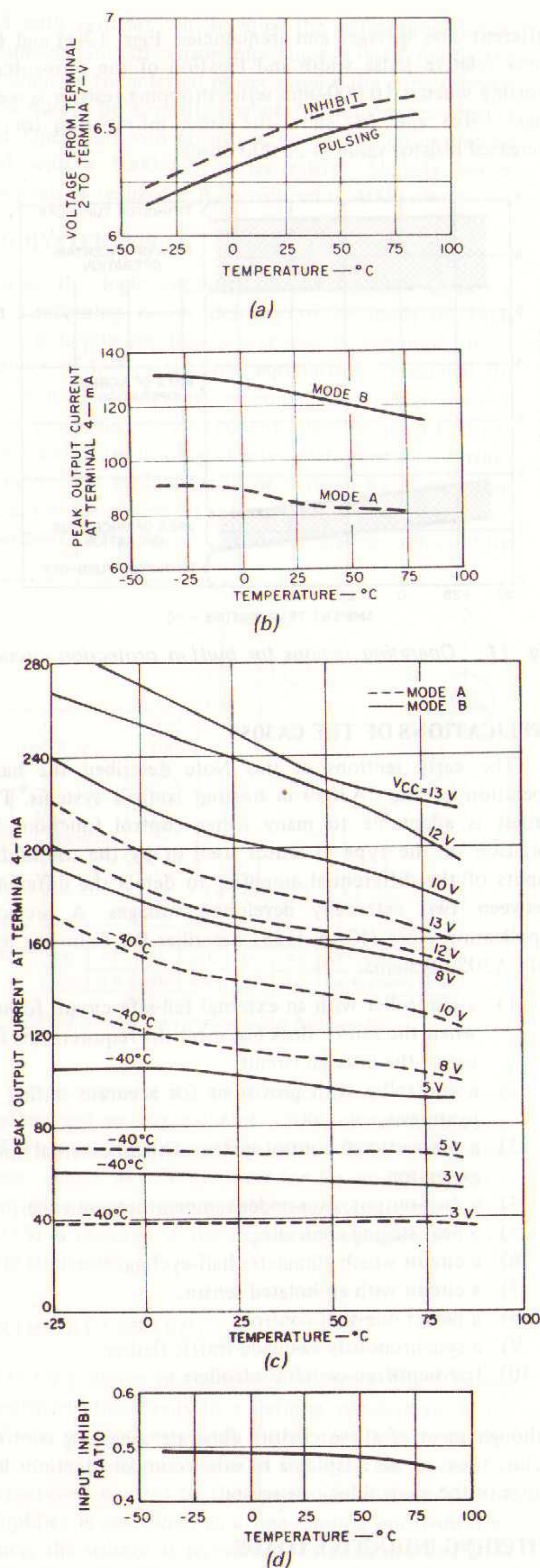


Fig. 12 - Characteristics curves of the CA3059 extended to cover the operating range from -40 to +85°C.

occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described in the published data for the CA3059. For highly inductive loads, however, this method is not suitable and different techniques must be used.

One technique is suggested in the circuit description section of this Note. If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero-crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI-eliminating function of the CA3059 is inhibited when the zero-crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

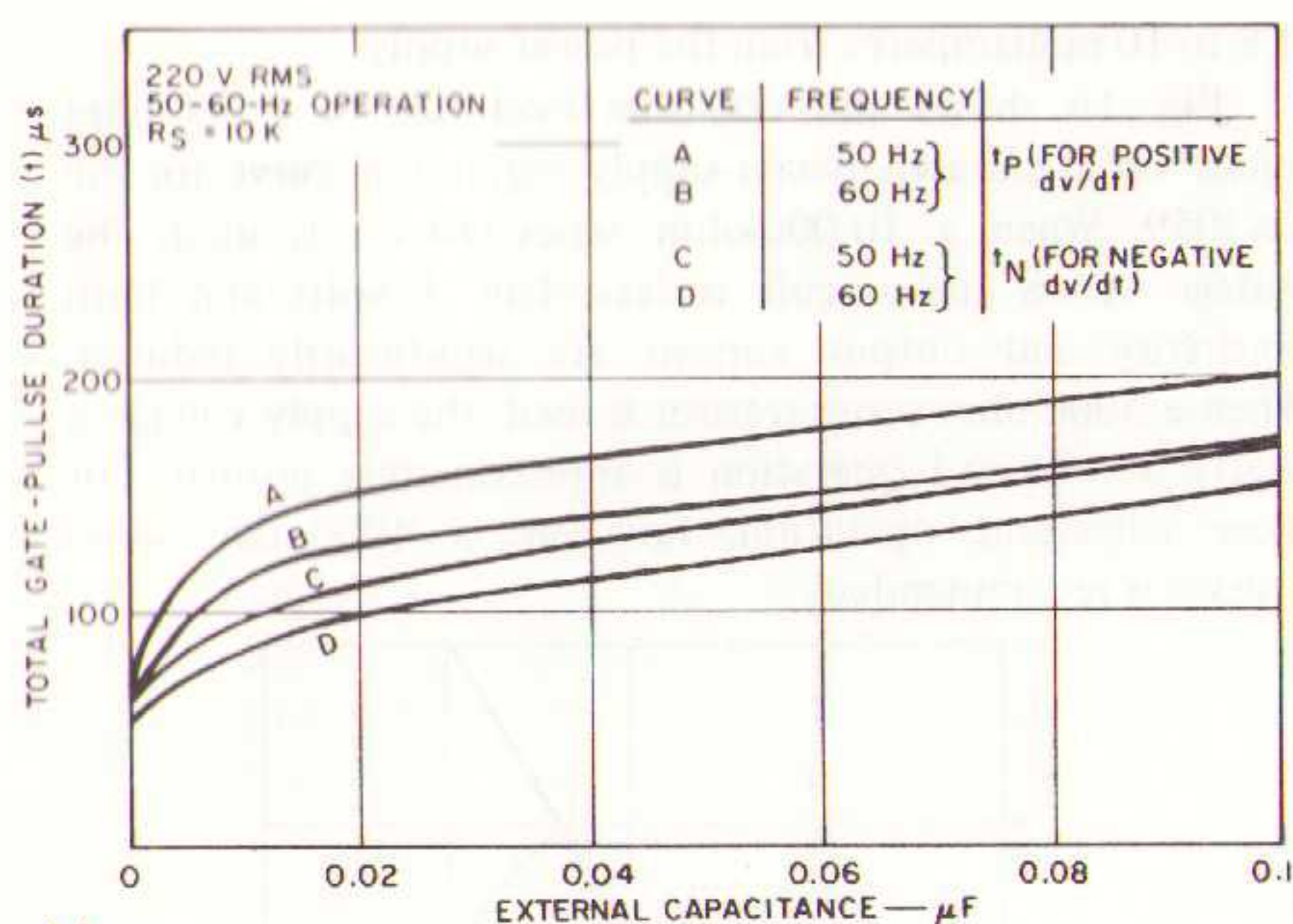
The limitation to this mode of operation is that the internal power supply cannot deliver a large average current; therefore, a sensitive-gate triac is required. Because these triacs have somewhat limited load-carrying capacity, this approach cannot be used universally.

The previous Note ICAN-4158 showed circuits which used a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

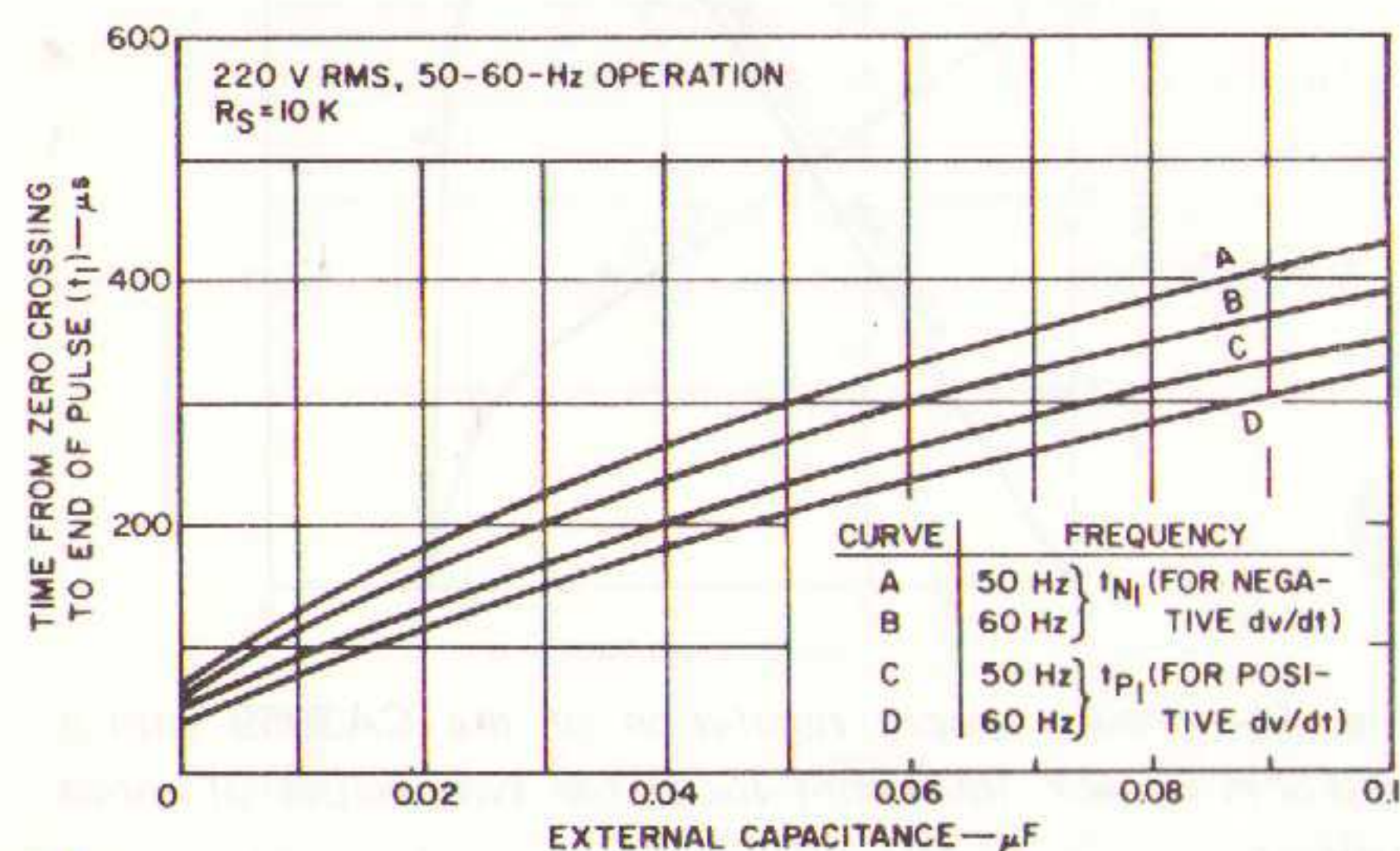
The circuit shown in Fig. 14 uses a CA3018 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops or 1.3 volts. When A is positive, Q3 and Q4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, Q1 and Q2 conduct. When the voltage at point A is less than ± 1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in R3 and output is inhibited.

The circuit of Fig. 14 forms a pulse of gate current in the manner described below, and can supply high peak drive to power triacs with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

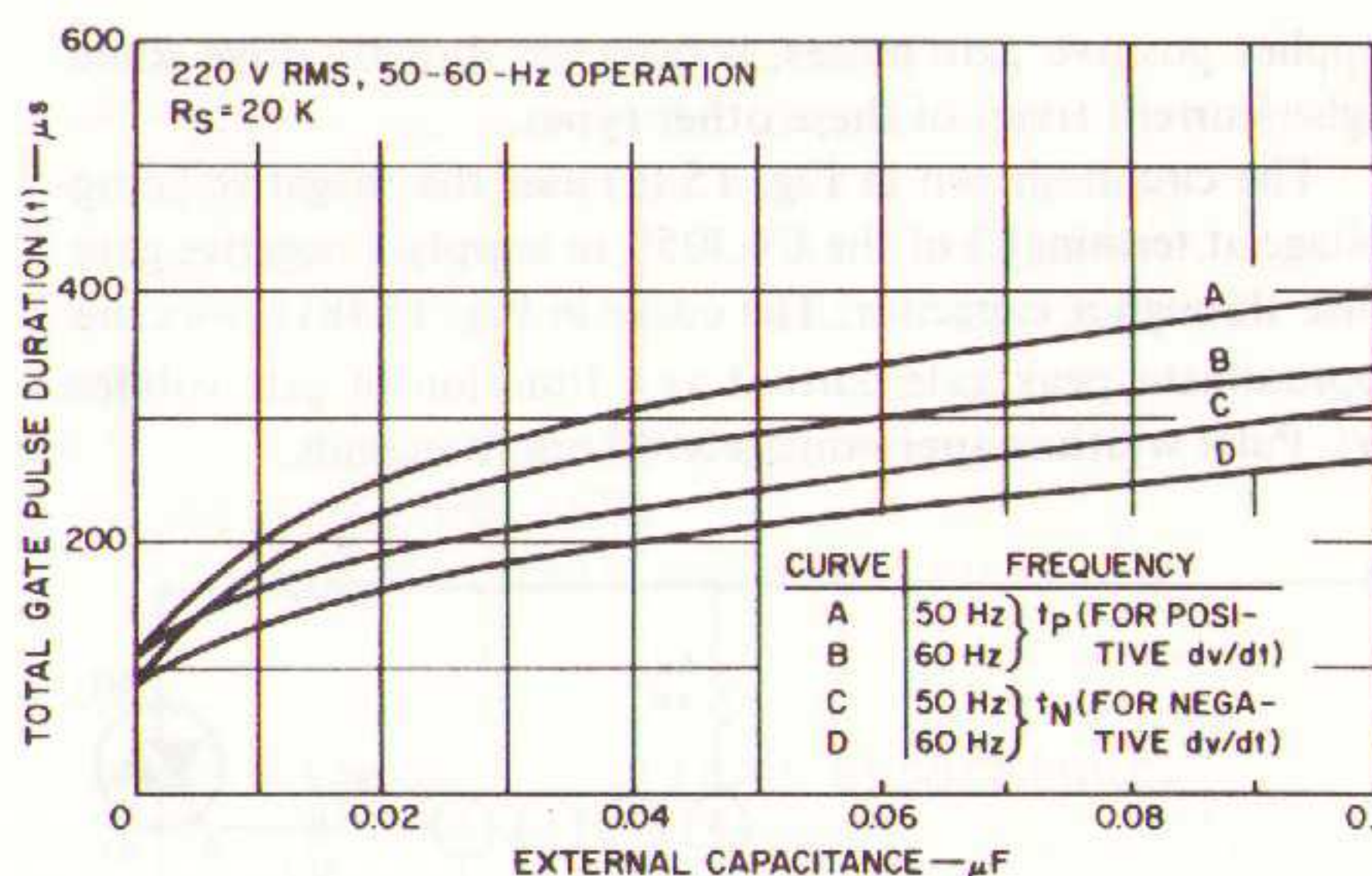
The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts; therefore, the



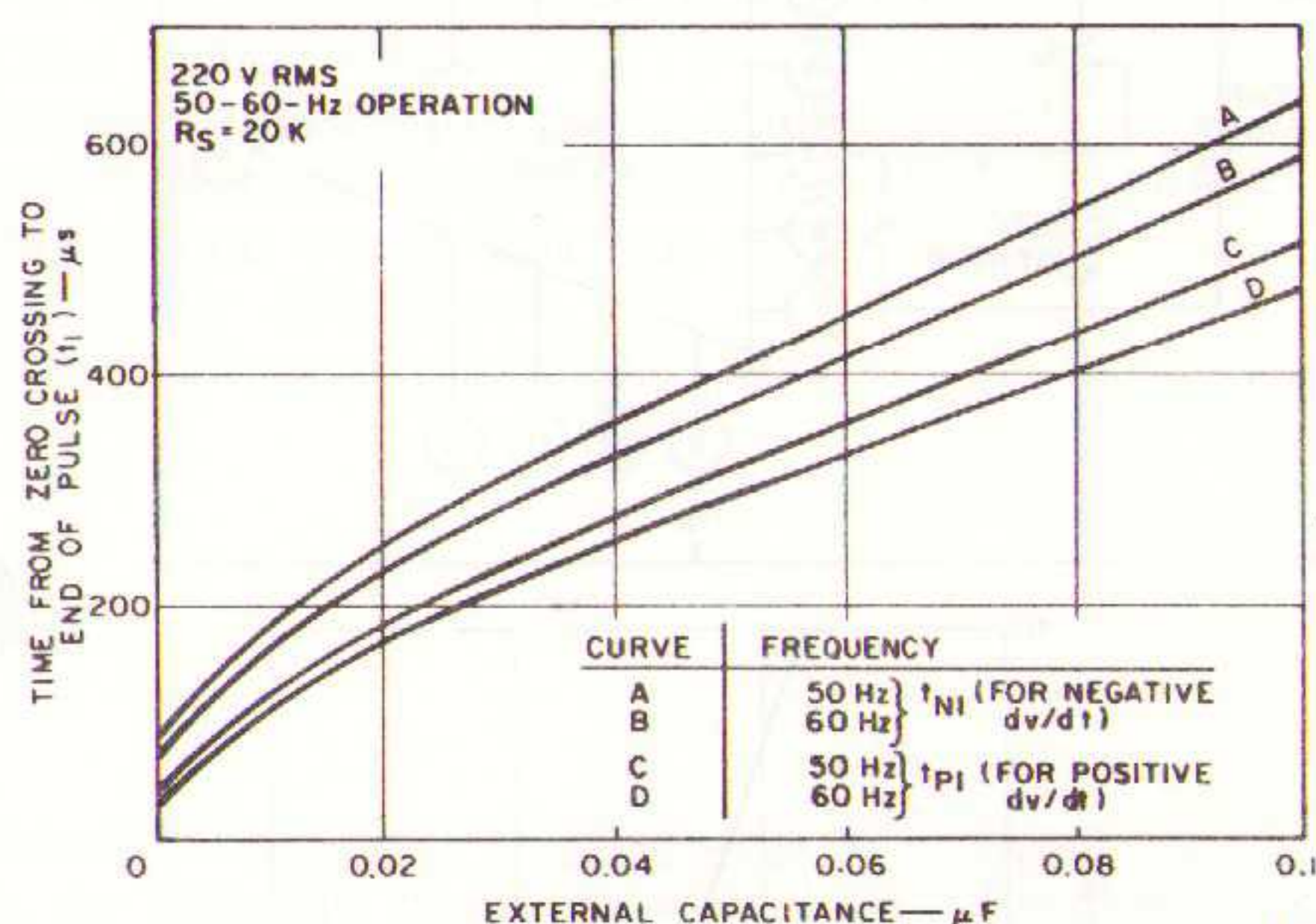
(a)



(b)



(c)



(d)

Fig. 13 - Relative pulse width and location of zero-voltage crossing for 220-volt operation.

output of the CA3059 is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage (v_T) of the thyristor. For most RCA thyristors, v_T (max) is less than 2 volts and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3018 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the holding current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

PROVIDING NEGATIVE GATE CURRENT

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I^+ and III^- modes). Sensitivity is degraded when the polarities are opposite (I^- and III^+ modes). Although RCA triacs are designed and specified to have the same sensitivity in both I^- and III^+ modes, some other types have very poor sensitivity in the III^+ condition. Because the CA3059

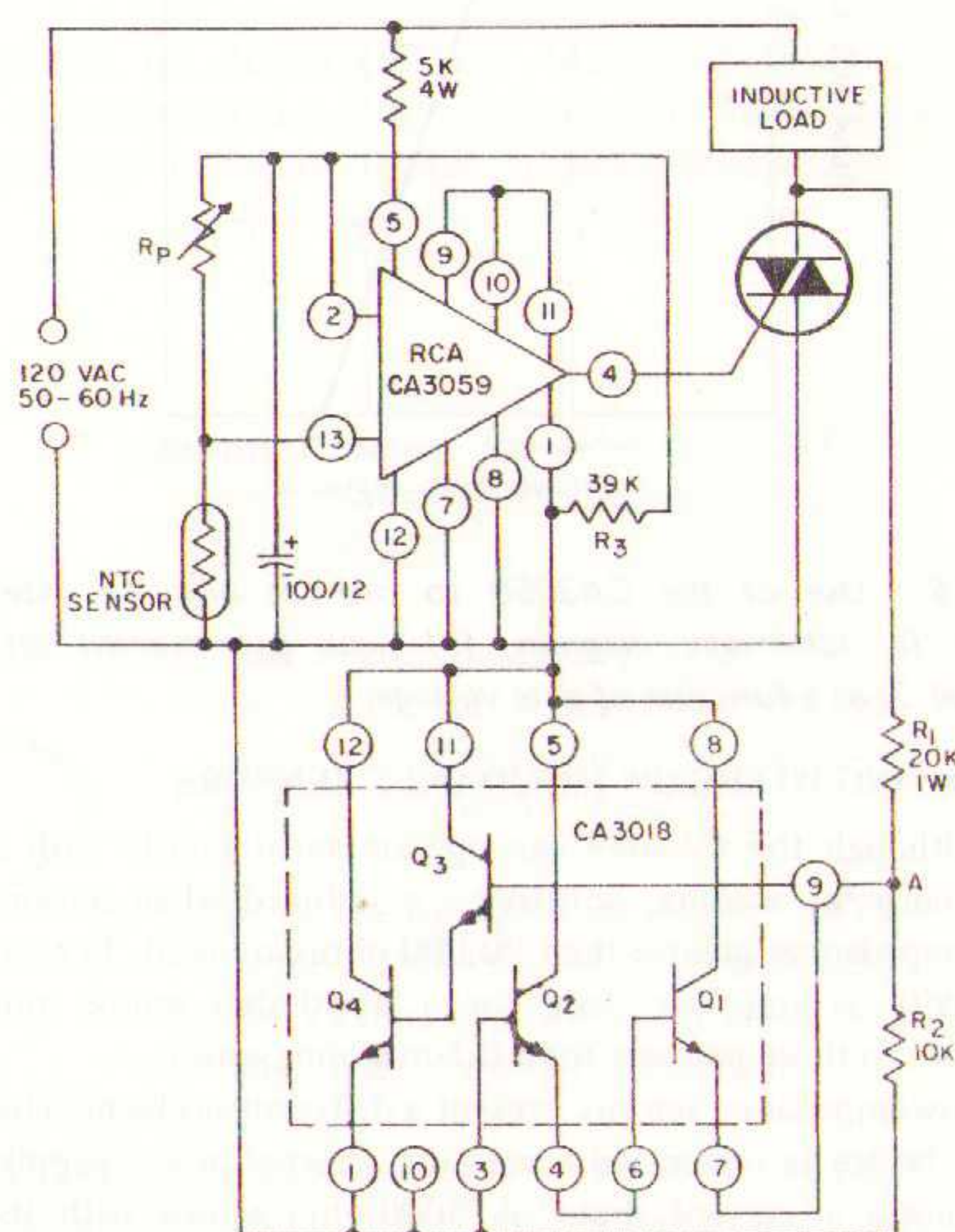


Fig. 14 - Circuit for switching inductive loads.

supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 15 (a) uses the negative-going voltage at terminal 3 of the CA3059 to supply a negative gate pulse through a capacitor. The curve in Fig. 15 (b) shows the approximate peak gate current as a function of gate voltage V_G . Pulse width is approximately 80 microseconds.

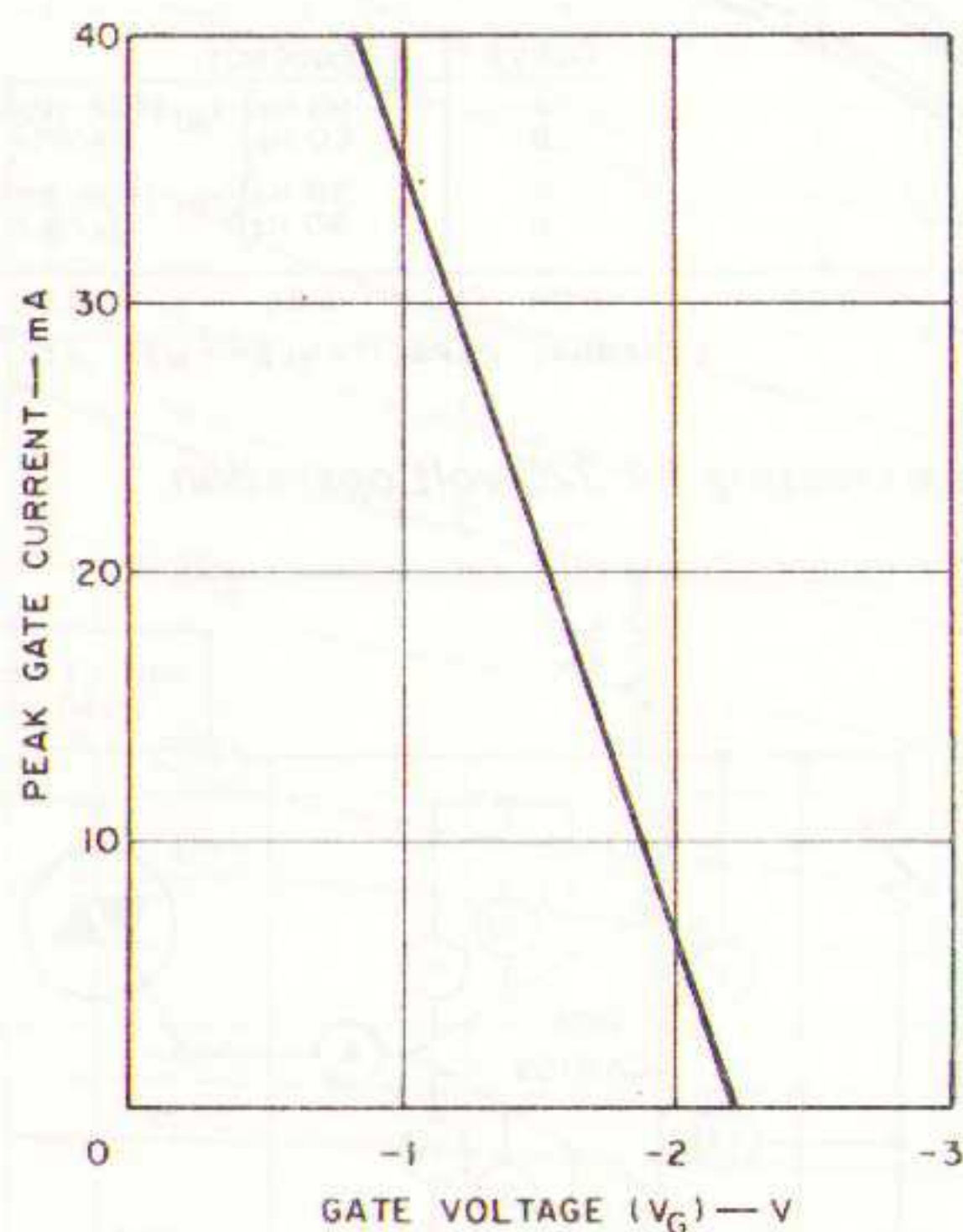
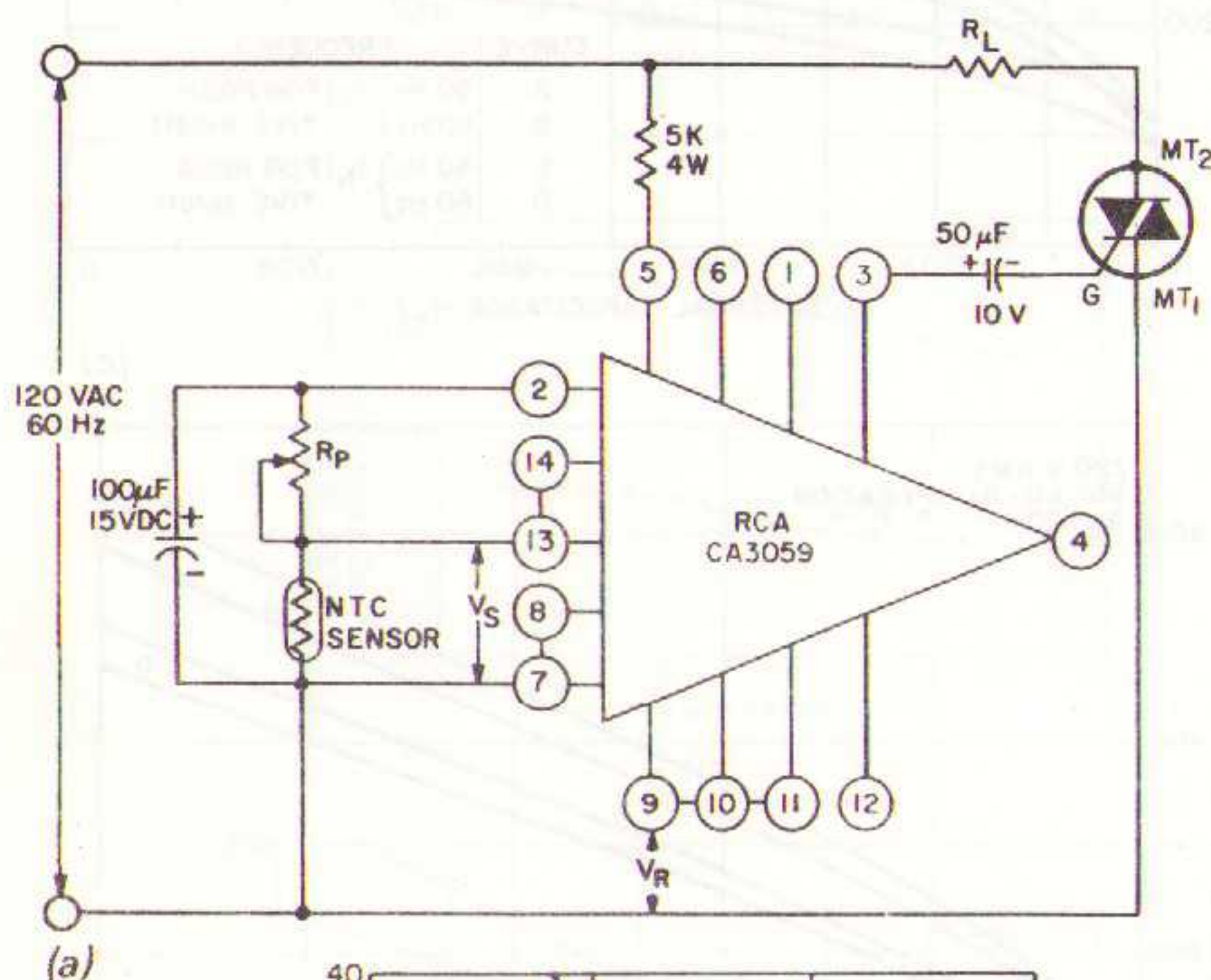


Fig. 15 - Use of the CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.

OPERATING WITH LOW-IMPEDANCE SENSORS

Although the CA3059 can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliamperes. On the other hand, a 300-ohm sensor draws a current

of 8 to 10 milliamperes from the power supply.

Fig. 16 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the CA3059. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

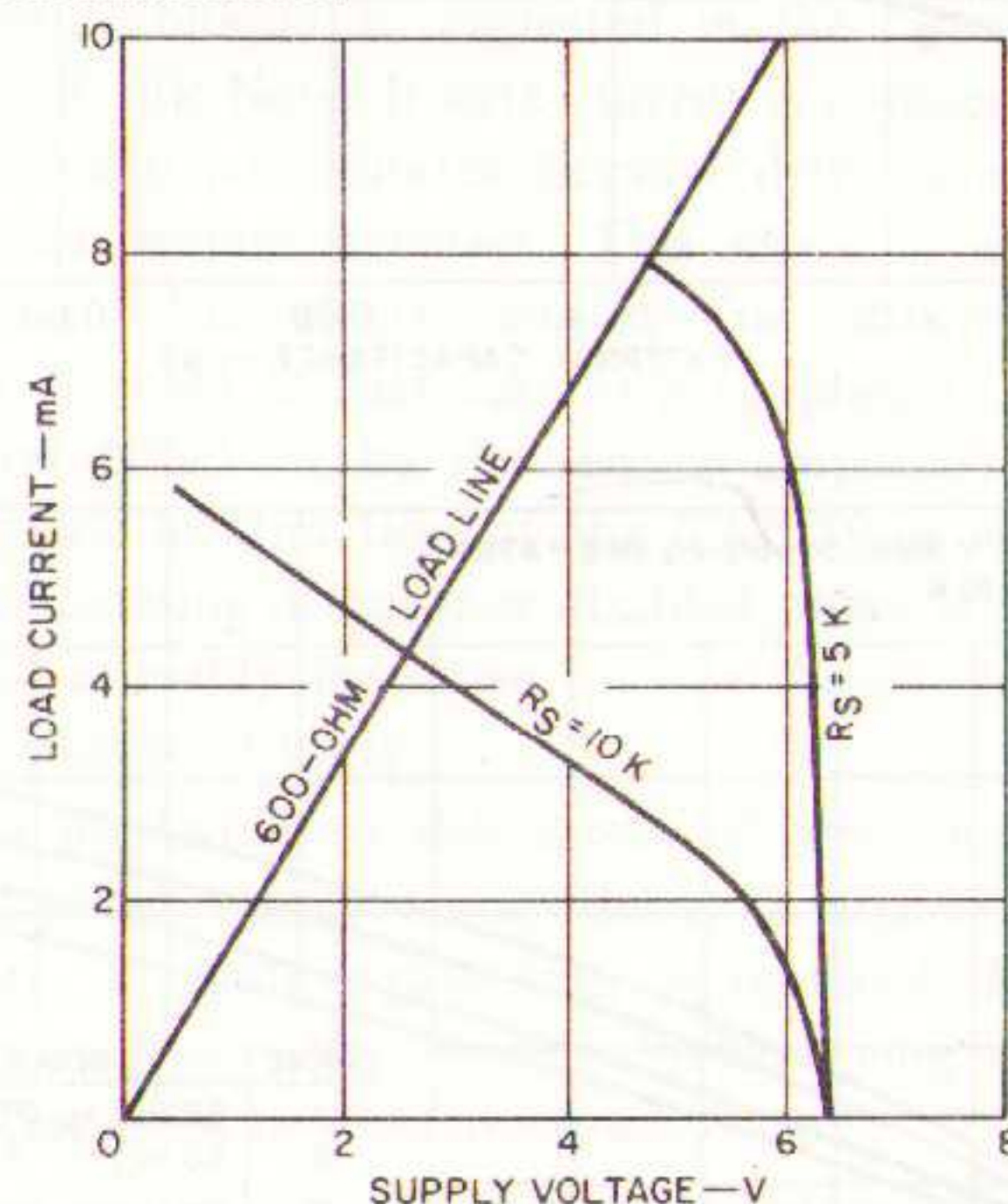


Fig. 16 - Power-supply regulation of the CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.

SYNCHRONOUS LIGHT FLASHER

The circuit shown in Fig. 17 is a simplified version of the system shown in the previous Note ICAN-4158. Flash rate is set by use of the curve shown in Fig. 10. If a more precise flash rate is required, the ramp generator described in the previous Note may be used. In this circuit, IC₁ is the master control unit and IC₂ is slaved to the output of IC₁ through

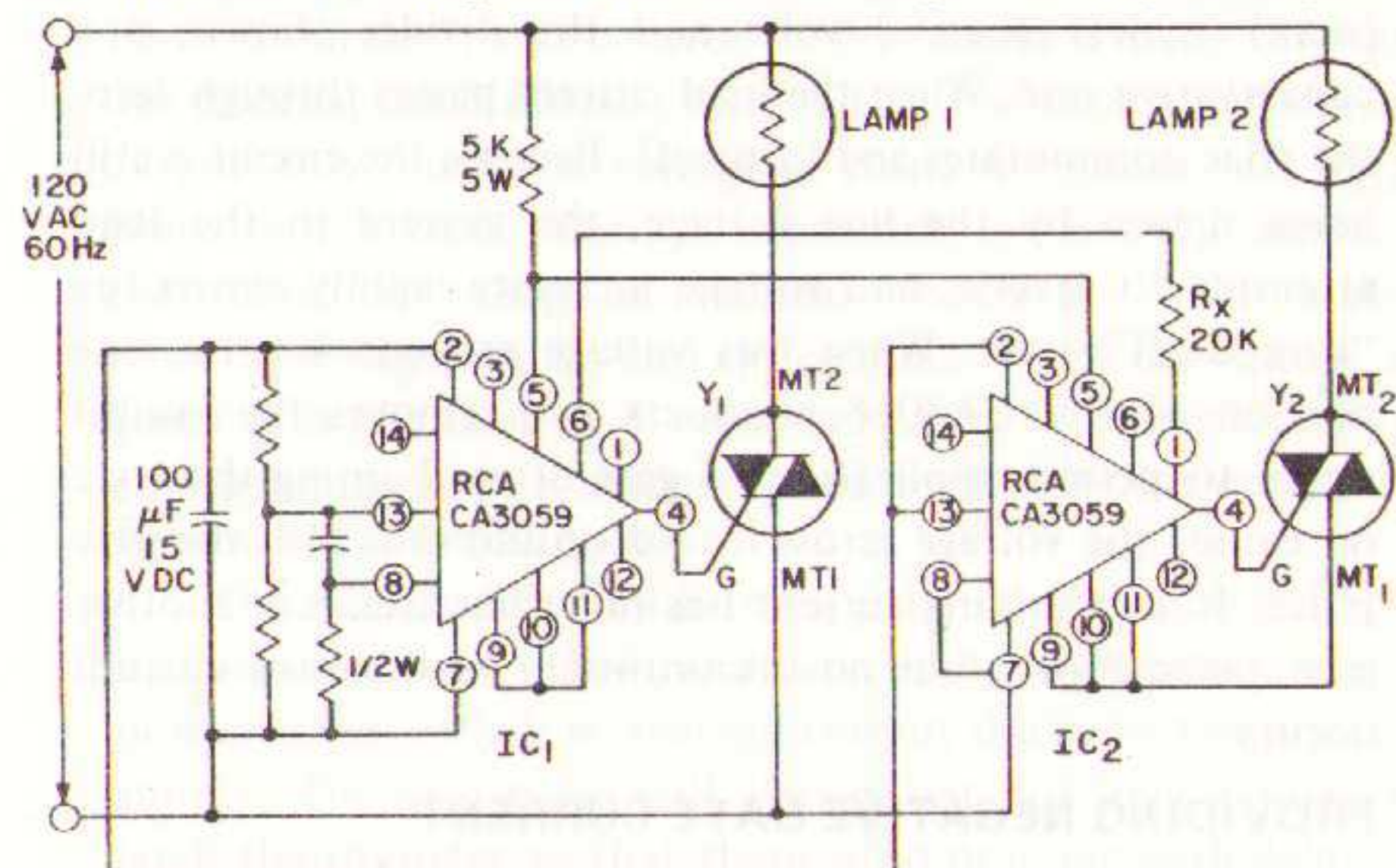


Fig. 17 - CA3059 synchronous light flasher.

its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on IC₁ is high and IC₂ is inhibited by the current in R_X . When lamp No. 1 is off, IC₂ is not inhibited and triac Y₂ can fire. The power supplies operate in parallel. The on-off sensing amplifier in IC₂ is not used.

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